LKP-1 MANUAL

Interak

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LKP-1 LATCHED PARALLEL KEYBOARD INTERFACE

USER MANUAL - ISSUE 2

Manual Price £2.50

PREFACE

This is a card produced especially for the Interak 1 computer, although of course it can be used in other systems.

It provides the interface between the user's ASCII (American Standard Code for Information Interchange) keyboard and the computer.

To the computer, this card looks like a single read-only port, which has 7 bits of ASCII data connected to the low order lines, with a positive strobe (indicating when the ASCII data are valid) connected to the highest order bit.

A special feature is that the data on the card are "latched" until they are read, which means that the computer no longer needs to be programmed to test the keyboard port continuously in order to avoid missing keystrokes. This can give similar performance to a keyboard which is interrupt driven but with much simpler hardware and software.

This card can be used in current Z80A systems as a functional replacement for the earlier 'Kemitron' DCR-6 keyboard interface card, and offers some significant performance advantages. It is also much more convenient to use the LKP-1 in a new system as it is bus compatible with other cards in the range.

Spare space on the card has partly been used to add a 4K "page" decoder, to suit very early 'Kemitron' cards which required such a circuit, but the main use in an Interak 1 system is to trigger a wait state monostable to provide wait states at selected locations in the memory map where relatively slow memory (such as EPROMs carrying firmware) may be located.

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ERRATA

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SPECIAL HANDLING REQUIREMENTS

Precautionary Notice

At this stage in the usual Interak 1 Manual a warning notice is presented telling of the dangers of damage to devices which are vulnerable to static electricity. The user of the LKP-1 card will be relieved to learn that no special precautions are necessary for the common types of LS TTL used on this card.

However the authors of this Manual were intrigued to read a report in a technical journal on the use of anti-static techniques in mass production of equipment in a factory environment. As expected the use of the correct techniques when handling static sensitive devices reduced the failure rate, but it was quite surprising to learn that the use of the same techniques on such devices as LS TTL (which were previously not thought to be static sensitive) resulted in a reduction of failure rate for these devices also.

There are newer high speed families of TTL becoming available (e.g. "ALS TTL", and "F TTL") and even though they are of bipolar construction, normally thought to be immune to static discharge damage, not MOS (metal-oxide-semiconductor), at least one manufacturer is recommending proper anti-static handling precautions because of the shallow diffusions used. A very exciting new digital logic family is the "74HC" range, and this certainly will need these handling precautions.

All of the above is mentioned here because it is expected that the LKP-1 card will have a fairly long lifetime, during which these new devices may be introduced, so the appropriate precautions are given here for completeness. Certainly it will do no harm to follow them as a habit whether you need to or not.

HANDLING PRECAUTIONS TO AVOID DAMAGE TO VULNERABLE INTEGRATED CIRCUITS BY STATIC DISCHARGE

Before unwinding any wire shorting together the pins of the ICs, or removing the ICs from their protecting metal or anti-static carrier tube, container, or anti-static foam, please read the following precautions:

1. Never use an isolated bit ("low leakage") soldering-iron to work on a circuit with the ICs in place. The bit should be earthed. If in any doubt, earth it by clipping on a small crocodile clip connected to earth. Similarly, all test equipment should be earthed before it is connected to a finished circuit.

2. Work on an earthed metal plate about a few feet square, (e.g. a stainless steel kitchen sink, or cooking foil), as a work-bench, when the time comes to install the ICs.

3. Keep all your tools on this earthed metal plate, and connect yourself to it, either by touching, or by using a piece of connecting wire formed as a wrist-strap. (Note: if you are using a wrist-strap, it is considered less hazardous to personal safety if the connection to earth is made via a 1 Megohm resistor.)

4. Before fitting the ICs, earth your circuit board, the IC sockets, and yourself; make sure that the power supply has been turned off and all electrolytic capacitors have been completely discharged.

5. Never leave unprotected ICs on a plastic or other non-conductive surface and never store them in ordinary white polystyrene without protection. (If a conductive tube or similar container is used, it is not possible for a damaging static potential to be built up inside such a container, nor could such a charge normally be introduced to the ICs from outside.)

6. Damage is less likely in humid conditions than dry ones. Try to avoid nylon and similar clothing, seating and carpeting, when working with these chips.

7. Use some form of IC sockets if you possibly can, as once the devices have been soldered, any guarantee which existed becomes void. If it is essential to solder the ICs, the supply pins should be soldered first, in order that the internal protection circuits have the maximum chance to carry out their task.

LKP1 LATCHED KEYBOARD PORT GENERAL FEATURES

* International Size Card (4.5" x 8", 114 x 203 mm)
* Suits Standard Parallel ASCII Keyboards.
* Keyboard data are latched on the card until read by the microprocessor.
* Generous "patch" areas provided for user's own purposes.
* In most cases can replace the "Kemitron" DCR-6 card.
* For special purposes a 4K page decoder can be added to trigger a "wait" state monostable, and/or provide a page select to early "Kemitron" cards e.g. VDU-A,B,G.
* In normal use needs no memory space at all, data appear at one I/O Port.
* Can also be used for other than ASCII data in special applications (e.g. input of keypad data, or control switch matrix).
* I/O Port number is completely selectable by means of links or DIL switches.
* Plated-through holes, Epoxy-glass PCB.
* Green Solder Resist on "A" side, (on "B" side also in some cases).
* Gold-plated edge connector on both A and B sides.
* 5V only operation.
* -12V is routed to the keyboard connection area, in case the user's keyboard requires -12V.
* ISBUS-A, INTERAK 1 bus compatible.
* KBUS-12 compatible. (Can be modified to KBUS-5 if -12V rail is not needed for the user's keyboard).
* Buffered where necessary to reduce bus loading to 1 "LS" load per line.
* No manufacturer's name appears on the card, thus ideal for OEM (Original Equipment Manufacturer) use.

2.1 INTRODUCTION

The LKP-1 is the interface between the user's own ASCII encoded keyboard and the Interak 1 system. An extremely simple and easy to understand technique has been used in the past (e.g. the 'Kemitron' DCR-6 card) for reading the keyboard. In essence the ASCII data are connected to the lower seven data bits of the keyboard interface. The eighth bit carries the strobe from the keyboard to indicate that the ASCII data are valid. The microprocessor continually reads the Keyboard port and examines the strobe bit, taking the data when they are valid.

Although it is very easy to understand and implement the method described above, it does suffer some drawbacks, which are eliminated in the LKP-1 design. The first drawback is that it is very easy for the computer to miss a keystroke if it is involved in some other activity and is therefore not examining the keyboard port often enough. The second drawback is that a deliberate delay has to be built into some software authors' programs to avoid the same keystroke being read more than once.

The features of the LKP-1 card which deal with the two drawbacks of the earlier method are as follows: Firstly the ASCII data from the keyboard are latched on the card whenever the keyboard strobe indicates they are valid. Therefore there is no danger that the keystroke will be lost, no matter how busy the microprocessor is when the key is pressed. Secondly, the action of the microprocessor reading the Keyboard Port results in the latch being cleared to all zeros (ASCII "null"), so that the same data cannot be read again, and special precautions no longer need to be taken in the software to prevent this.

Non-Interak 1 Uses

The circuit so far described is all that is necessary for this card to fulfill its function in an Interak 1 system. However, as there was some spare space on the card some extra circuitry was added to suit the needs of users of other systems, using for example early "Kemitron" cards.

In particular, the "Kemitron" equivalent of the VDU-K is a three card set known as VDU-A,B,G. The VDU-A,B,G set is not compatible with any of the buses used for this size of card. Also, the cards have decoding for only a 12-bit address, and so they need a 4K "page select" signal. A 74LS154 device is fitted on the LKP-1 card to provide this page select in such a system.

Wait States

There is no need for any action to be taken in providing "wait" states for the LKP-1 card in its normal operation; it can cope easily with the Z80A timing for I/O transactions right up to the full 4.0 MHz CPU clock frequency.

However the subject of "wait" states has been introduced here for another reason:

Normally there is no need for EPROM cards in the Interak 1 system, since it is predominantly RAM-based. As the RAM can work without "wait" states, at the full 4.0 MHz CPU clock frequency, then there is normally no need to slow the processor down at all. However, one of the features of the Interak 1 system is its modular nature, and the LKP-1 card could easily be used within an Interak 1 system which had a large complement of extra cards (e.g. EPROM programmer etc. etc.) which may need memory access "wait" states to be added. Or perhaps the LKP-1 card could be used in a very small dedicated application computer, where a single EPROM/RAM card would provide all the memory requirements. In both these examples, it may become necessary to incorporate "wait" states into certain memory accesses, especially those for the EPROMs, as they may be too slow for a Z80A running at its full 4.0 MHz.

The logically correct location for the "wait" state circuitry is for it to be provided on those individual cards for which "wait" states are required.

However, advantage has been taken of some spare space on the LKP-1 card, which would otherwise have been wasted, and the fact that track has been laid out for a 4K Page decoder to suit very early "Kemitron" cards (see "Non-Interak 1 Uses" above), to provide for an optional "wait" state on any of 3 chosen 4K pages in the memory map.

Another use for "wait" states, which is perfectly valid in an educational environment, is to use them purely as an example of the technique used, for the benefit of students learning about the Z80A. The appropriate waveforms can be displayed on an oscilloscope, and the action of the "wait" line demonstrated most clearly, by varying the duration of the monostable which requests the "wait" state(s).

General

All of the components used are readily available. The integrated circuits used are all laid out the same way round, which makes the card very straightforward to construct and test. Wherever possible signal tracks which have to pass between the legs of ICs are taken on the A-side so that they can be inspected in case of trouble. (Less considerate designers take them on the B-side where any shorts will be hidden under the IC sockets!) Plated-through hole construction is provided, and a solder resist mask on the A-side (some recent issue cards have a solder resist mask on the B-side also).

Although all of the signals are taken via the A-side of the 0.1" pitch edge connector (which is gold-plated) a gold-plated edge connector is also provided on the B-side.

Contents of Kit

The kit of components, which is sold separately to the p.c.b. itself includes 9 resistors, 2 SIL resistor packs, 1 variable resistor, 13 capacitors, 1 diode, 10 integrated circuits, 11 integrated circuit sockets (one of which is provided for an optional DIL selection switch), and some 0.1" pitch pin assemblies.

A 1" metal card front is recommended but is not included in the kit to keep the basic cost down for those working to limited budgets. Also excluded from the kit but required is a 20-way ribbon cable connector for the keyboard connection. (The connector has not been included because the exact type and style will depend on the user's wishes, and whether or not a front panel is fitted.) A further option is a DIL switch, which can be used for altering the port address quickly if required, however most users will not require to change the address once it is set, and thus will not be able to justify so easily the cost of providing this component.

2.2 LKP-1 CARD GENERAL DESCRIPTION

The LKP-1 card is part of an Interak 1 system and provides the means for the user to enter data into the computer. Although some other type of keyboard (such as a "hex. keypad") could conceivably be connected as input to the LKP-1, the normal input will be ASCII encoded data from a full "QWERTY" keyboard (i.e. like a type-writer keyboard) having perhaps 50 keys or more.

The ASCII (American Standard Code for Information Interchange) is a seven bit code which is an ideal standard for this kind of application, since it is universally known and recognised. It is a seven bit code, which permits 128 different combinations, enough for all the letters of the alphabet, both upper and lower case (i.e. capital letters and small letters), the numbers, punctuation marks and so on. There are a number of codes which are known as "control codes"; these are for such functions as "back-space", "tab", "carriage return", "line feed", and so on. The names for many of these codes betray their early origins, as controls for equipment like Teletype machines; on some modern computers there is no such thing as a "carriage" to be "returned" (if it has to be returned by midnight it sounds a bit like something belonging to Cinderella, but that's another story), nevertheless the terms are so well established that they can't be changed. Another code which captures the imagination is hex. 1B, the code for "escape".

The computer determines which key is being entered on the keyboard by reading a chosen "Port" in the I/O space of the computer, a Port to which the keyboard is connected. In the Interak 1 computer the Port chosen is 40H. (The suffix "H" means the Port number is in hexadecimal notation. The word "hexadecimal" is often abbreviated to "hex.", as used earlier in this Section of the Manual. Note that "hex." (with the full stop), short for "hexadecimal", is not the same as "hex" (without the full-stop); "hex" means six.) However, back to the plot:

It is possible, but not certain, that when a particular key is pressed all seven (ASCII) bits will change simultaneously. If the computer happened to read the Keyboard Port when the data were changing there is therefore a chance that it might recognise a code for some other key, which circumstance is of course not desirable. Another problem which it is essential to overcome is that of the inability of the computer to distinguish between say a repeated key "A" (i.e. pressed twice in quick succession), and a single key pressed once and held down.

Needless to say there is a recognised technique for dealing with these potential sources of difficulty. Extra hardware is added (by the manufacturer of the keyboard, or the manufacturer of the IC(s) used) to provide a signal known as a "strobe". The strobe signal is only activated when the ASCII data from the keyboard have been established for the particular key pressed, and has had sufficient time to be guaranteed stable. The strobe can also be used to help the computer

distinguish between the two successive key "A"s (in the above example) and the single key "A" held down. In the former case two strobes are produced, and in the latter only a single strobe.

Types of Keyboard

The requirements for a suitable type of keyboard for the LKP-1 card are largely defined by those outlined above. In summary, the keyboard has to provide 7-bit ASCII encoded data, and a strobe.

In the Interak 1 computer the 7-bit ASCII data are connected to the low order data lines: bits 0 to 6. (Bit 0 has the least significant bit of data, and bit 6 the most significant bit). The strobe is connected to the most significant bit, bit 7. At the data bus of the computer the ASCII data have to be active high, e.g. code 00H, "NUL", should appear as seven "low" bits, codes with 1's present should have the appropriate bits set "high". The strobe should also be active high, i.e. if the lower seven bits contain valid data, the eighth (most significant bit) should be "high". One way of looking at the software which suits this arrangement is to see it as testing whether the data byte at Port 40H is positive or negative. One convention for dealing with 8-bit "bytes" such as are received from Port 40H, is that numbers with a "1" in the high bit are negative, numbers with a "0" there are positive. Thus a negative number indicates that valid data are available, a positive number indicates they are not. (Note that there are other conventions for dealing with binary numbers; this is just one way of looking at the software needed, given to indicate the "flavour" of the method, by way of introduction.)

There are a number of variations possible within the framework of a design for an ASCII encoded keyboard with strobe, which suit the convenience of the particular keyboard manufacturer, and the LKP-1 card has been designed to cope with the more common variations.

Examples of typical variations encountered are as follows:

The ASCII data can be exactly as the code dictates, or they may be totally inverted (i.e. all 0's changed to 1's and vice versa). The standard LKP-1 card and components expect conventional non-inverted ASCII data, but the inverted data can be accommodated by replacing the non-inverting buffer chip on the card with an inverting type.

The keyboard outputs can be standard "TTL" (Transistor-Transistor Logic) levels, or they can be "open collector". In the latter case pull up resistors are needed, and needless to say are provided on the LKP-1 card and in the kit of parts. It generally does no harm, and often increases the "noise immunity" of a circuit, to provide pull up resistors even when they are not being driven by open collector outputs, which is the reason they are provided as standard on the LKP-1 card. (If they are driven by TTL "totem pole" drivers the resistors can be looked on as being "line terminating resistors" rather than pull-ups; it is best to leave them installed if you can so that the card will suit the widest range of keyboards without modification.)

The strobe can be any of four types: positive edge (i.e 0 to 1

transition indicates valid data), negative edge (i.e. 1 to 0), positive pulse (data valid on both leading and trailing edges of a short logic 1 pulse, strobe line low when no valid data available) or negative pulse (data valid on both leading and trailing edges of a short logic 0 pulse, strobe line high when no valid data available). Selection links are provided on the LKP-1 card to suit any of these arrangements.

Latch

A latch is included in the Keyboard Interface Circuit. The main purpose of the latch is to relieve the CPU of the chore of having to examine the Keyboard Port continually, so as to avoid missing a key. With the latch it is only necessary to examine the Keyboard Port at relatively infrequent intervals, since the keyboard data are stored in the latch until they can be read by the CPU. It is the strobe itself which writes the keyboard data into the latch, and it is the action of reading the keyboard which clears the latch ready for the next keystroke. The operation summarised in the last sentence makes it easy to write software which can avoid reading the same key twice (which results in some keyboards in well-known but non-Interak systems being unfairly criticised for having "key bounce" problems, when in fact the trouble is the software, or the keyboard interface design). No matter how quicky the software comes round to read the port again, the data will have been cleared by the successful read of the data the first time. Using this method it is necessary for the circuit to include some logic to cater for the very rare occasion when the CPU happens to begin its input from the port at the precise moment when the data from the keyboard are about to change; without this extra logic there would be an outside chance that the data might be cleared from the latch although they hadn't been read properly.

4K "Page" Decoder, and "Wait" State Monostable

This circuit has nothing to do with the Keyboard Interface part of the card. It is included on this card to utilise spare space which would otherwise be wasted, and to save the user the cost of an extra card to accommodate this circuit should it be required.

The need for a 4K page decoder is a left-over from the very early cards in the original "Kemitron" range (from which all that we see today was derived). Some of the early cards permitted partial address decoding, the data bus contention (which would otherwise have resulted when more than one card responded to a given address) being prevented by issuing each affected card with one or more 4K "Page Select" signals. The method is not used in the current Interak 1 system, because it breaks the fundamental rule "any card in any slot". The card in the Kemitron System which provided the page select signals was the keyboard interface card, type DCR-6, and it is that card which has been superceded by the LKP-1 card. (See Section 4.5 of this Manual for more details of the DCR-6 card.)

The most common requirement for a 4K page select in the early Kemitron System was for the VDU-G card of the three card VDU (VDU-A,B,G). The Interak 1 single card which can be used to replace the three earlier

cards is VDU-K; this includes as one of its features full address decoding, and thus does not need a page select signal. The 4K page decoder on the LKP-1 card is used mainly to save the Kemitron VDU-A,B,G cards from becoming obsolete should the user change his Kemitron DCR-6 for the Interak LKP-1.

As a bonus, the provision of a 4K address decoder on the card turns out to have some use in an Interak system. One is for applications of the card which require it to be located in the memory space of the computer rather than its natural location in the I/O space; some of the extra address decoding required is thus already present. (See Section 4.3 of this Manual for Applications such as this). Another, and in fact the most likely current use, is to act as a trigger for a monostable which is connected to an open-collector driver for the "Wait" line on the bus. Although the Interak 1 system is predominantly RAM-based, and can work at 4.0 MHz with no wait states, it must be slowed down slightly using wait states whenever slow memory such as EPROM is being accessed. Strictly speaking the logical place to put this circuitry is associated with the slow memory devices themselves, but this would result in the wait state circuit being duplicated at several locations within the system. Nevertheless it is likely that new cards will have wait state circuitry where appropriate, but in the meantime the circuit on the LKP-1 will be a very convenient source of any wait states which are needed.

Examples of places in the system where EPROMs are, or may be, used are: the on board EPROM on the MZB-3 CPU card, the EPROMs which would be used for other resident firmware, such as BASIC in EPROM, and of course an EPROM copier/programmer. Up to three chosen 4K pages may be wired in directly to the wait state circuit, and these will usually correspond to the three examples of EPROM usage given. There are two generous "patch" areas on the LKP-1 card, and these may be used to incorporate circuitry for wait states for more of the 4K Pages if required.

Port Address

The Port Address is selectable so that more than one LKP-1 card can be used in a system for some special purpose, for example to permit a control panel of some description to be fitted, or perhaps to use the card as a simple 7 or 8-bit Input Port. (See the Applications Section in Appendix 4.3 of this Manual).

This concludes the General Description of the LKP-1 card.

2.3 DIL SWITCH SETTINGS, LINKS, OPTIONS, etc.

DIL Switch S1a-h

There is one position (labelled S1) on the card where a DIL switch may be fitted. A DIL switch is not supplied in the standard kit of parts as it is a fairly expensive component and many users will prefer to make other arrangements. However a DIL socket for S1 is supplied. (Strangely many people do not use sockets for DIL switches even though being mechanical components they are more likely to fail than ICs, and every bit as hard to remove once soldered.) As an economy measure, a cheap method of making the necessary connections without suffering the permanence of soldered wire links is to strip some short lengths of single strand insulated wire (not too thick otherwise there is a risk of damaging the socket), bend them into hoops, and push them into the socket provided for S1. However, for the purposes of this description it will be assumed that a DIL switch is used.

The type of DIL switch to be used is 8 x SPST. We can therefore refer to eight switches S1a to S1h; oriented so that S1a would connect pins 1 and 16 of the socket, if the pins were counted in the same way as for a 16-pin I.C.

The switches S1a-S1h select the I/O Port address. This will have to suit whatever software is in use; the settings for Interak 1 are given at the end of this paragraph. S1a is the MSD (most significant digit) and corresponds to the state of address bus line AB7; the other switches continue in sequence until S1h is reached, which corresponds to AB0. Note that due to the fact EX-OR gates are used to select the chosen address (see circuit diagram Sheet 2), the complement of the address should be set on the switches, i.e. for an address with a "1" on a given line, the corresponding switch should be set to "0", by turning that switch ON. For example for use in an Interak 1 system with a ZYMON 2 monitor, the Keyboard Port is 40H. In binary notation this is 0-1-0-0-0-0-0-0, and so the required settings for S1a to S1h are OFF-ON-OFF-OFF-OFF-OFF-OFF-OFF respectively. Note that as this means that only one switch needs to be closed, there is no real need to purchase a full 8 x SPST type, one with less switches will do just as well in this application.

Choice of Non-Inverted or Inverted Data Inputs

The preferred keyboard input is non-inverted data, i.e logic 0 represented by a "low" voltage, and logic 1 represented by a "high" voltage. If this is the case use the standard non-inverting octal data bus buffer (type 74LS244) supplied in the kit of parts for use in position U9.

Some keyboards for one reason or another are able to provide only inverted data outputs. Such keyboards can be accommodated by making a simple component change on the LKP-1 card. To suit inverted data inputs an inverting type of octal data bus buffer, i.e. type 74LS240, should be fitted in place of the standard type normally used in position U9.

(The keyboard strobe follows a different circuit to the ASCII data on the LKP-1 card, and so the choice of a non-inverting or non inverting buffer for U9 is not influenced directly by the type of strobe provided by the keyboard.)

Selection of Input Pull-up Resistors

Eight 1k pull up resistors are provided in the shape of the SIL resistor pack SIL1. They pull-up the seven ASCII data input lines and the strobe input.

1k is a suitable value for either open collector drivers or TTL level outputs on the keyboard. (In the latter case they are not really needed but may be some use in acting as terminating resistors to improve the immunity to noise on the relatively long keyboard input cable.)

As the majority of parallel ASCII coded keyboards conform to one or other of the two general types implied in the last paragraph no attention is normally required to SIL1.

In rare cases the strobe output is different to the ASCII data outputs from a keyboard, and in such a case it will be found convenient that this "odd one out" is pulled up by the very last resistor in the SIL1 resistor pack. If for example the strobe line for some reason did not need a pull up resistor and all the other lines did, an 8-pin resistor pack could be substituted for the 9-pin type supplied in the kit, or the 9th pin could be cut off, or the 9th pin of the mating SIL socket could be omitted. (If on the other hand the strobe line was the only one which required a pull up resistor, then the whole SIL pack could be removed, and a single discrete resistor fitted across pins 1 and 9 of the old SIL1 position.)

Some rare keyboards are incapable of driving the loads associated with normal TTL levels, and might be unable to provide a satisfactory logic 0 when battling against the opposing 1k pull up resistor(s). In such circumstances it is a simple matter to remove and discard SIL1 entirely (the kit of parts provides sockets for the SIL packs so as to make it easy to remove and/or replace them).

0.1" Pitch Pin Assemblies

There are eight groups of these, marked on the diagrams as P1 to P8, although for the convenience of packing the kit each group may be made up from a number of individual assemblies, e.g. a 10-pin group may be made up from two 5-pin assemblies.

All of the IC's, DIL switches, and SIL resistors, are mounted the same way round, i.e. with all pins 1 towards the same edge of the card. The numbering of each group of pin assemblies should be taken as following the same convention. As a reminder pin 1 of each group is marked on the component overlay diagram towards the back of this Manual.

The pins are used as test and/or termination points. In the latter case it is intended that the very useful technique known as "wire-wrapping" be employed. A wire-wrapped joint can be made with a small hand tool, about the same price as a soldering iron, and makes a joint without heat which is equal to or better than a soldered joint in reliability, and most importantly can be removed just as easily. It has been chosen here for two reasons. Firstly so that installation work can be carried out on the computer without the need to use a soldering iron, and secondly so that the settings can be altered repeatedly without damaging or marking the card in any way. (This is important because of the anticipated long lifetime, long for a computer anyway, of several years. During that length of time repeated soldering and desoldering would soon take its toll on the card connections.) If you do not have suitable wire-wrapping equipment then you can make the connections in some other way, even soldering them if you must.

The various functions of the groups of 0.1" pitch pin assemblies are discussed next:

P1 and P2

These are optional connection points for connecting a front panel 20-way ribbon cable connector. There is space on the card for an alternative p.c.b mounting connector which can be used instead if no front panel is to be fitted. In either case P1 and P2 make useful test points. If they have been installed neatly a 20-way ribbon cable connector can be pushed onto them; this is very useful for test purposes if a card has to be tested when the customer has used a non-standard connector.

The recommended connections for the front panel type of connector are exactly the same as would be made naturally if the p.c.b. type of connector was used; they are indicated diagramatically on sheet 3 of the Circuit Diagram in Section 5.4. The connections are also presented below for the convenience of the reader:

	P1	P2	
N.C.	1	1	B0
N.C.	2	2	B1
N.C.	3	3	B2
N.C.	4	4	B3
N.C.	5	5	B4
N.C.	6	6	B5
Strobe STB	7	7	B6
-12V	8	8	(B7)
+5V	9	9	+5V
0V, Earth	10	10	0V, Earth

The above pin assembly identifications translate to the following ribbon cable connections:

Ribbon Cable Connector Viewed From Rear (Inside) of Front Panel

top

	B0	19	20	N.C.
	B1	17	18	N.C.
	B2	15	16	N.C.
	B3	13	14	N.C.
"P" indicates	B4	P 11	12	N.C.
polarisation	B5	P 9	10	N.C.
slot position	B6	7	8	Strobe STB
	(B7)	5	6	-12V
	+5V	3	4	+5V
	0V, Earth	1	2	0V, Earth

The following diagram gives exactly the same information, but this time viewed from the other side of the front panel.

Ribbon Cable Connector Viewed From Front (Outside) of Front Panel

top

N.C.	20	19		B0	
N.C.	18	17		B1	
N.C.	16	15		B2	
N.C.	14	13		B3	
N.C.	12	11	P	B4	"P" indicates
N.C.	10	9	P	B5	polarisation
Strobe STB	8	7		B6	slot position
-12V	6	5		(B7)	
+5V	4	3		+5V	
0V, Earth	2	1		0V, Earth	

Note 1. No connection should normally be made to pins 5, 10, 12, 14, 16, 18, and 20 of the ribbon cable.

Note 2. Some keyboards provide more than 7 bits of data, and have for example a parity signal, shown as (B7) above, on their eighth output line. It should be ignored, as the strobe signal STB is required on the eighth data line in an Interak system.

Note 3. Some keyboard manufacturers number their data output lines as B1 to B8, instead of the numbering shown above (B0 to B7).

Note 4. Some ribbon cable manufacturers allocate the numbers for the ribbon cable as 20 to 1 instead of 1 to 20. If in doubt use the polarising slot to establish the correct numbering (it is on the same side of the connector as the odd-numbered pins). Note also that the coloured stripe often found on grey ribbon cable is usually the pin 1 cable identifier.

Wire-wrapping is a recommended method of connecting the ribbon cable

plug to the LKP-1 card. Another method is to use push on crimped connectors, or even, if you have no alternative, soldered connections directly to the pin assemblies.

P3 and P4

These are the connection points for the sixteen 4K Page Select outputs from U1. They are laid out on the card as follows:

	P3	P4	
PS0	1	-	
PS1	2	-	
PS2	3	-	
PS3	4	-	
PS4	5	-	
PS5	6	-	
PS6	7	-	
PS7	8	1	PSF
PS8	9	2	PSE
PS9	10	3	PSD
PSA	11	4	PSC
	-	5	PSB

(The Page Select signals PS0 to PSF are given above in hexadecimal notation, and should really be marked with a bar above each name, as they are "active low", i.e. they go low to select the 4K page.)

The Page Select signals may be used for any purpose of the user, but often three are selected to provide three inputs for the wait state controller, see "P5" next.

P5

P5
1
2
3

This is a three pin assembly which provides three inputs to the wait state controller. They can be left unconnected if no wait states are desired; or connected to any signal which exhibits a negative going (1 to 0) transition when a wait state is required. Commonly one or more of the inputs are connected to chosen 4K page select outputs taken from P3 and/or P4, as discussed above. The three inputs are interchangeable, and may be connected in any convenient order. However the physical layout on the board positions them so that they are adjacent to the three most likely page select signals in an Interak 1 system, i.e. PSC, PSD, PSE.

Specific instructions for connections to P5 in an Interak 1 system are as follows:

Connect P4 pin 2 to P5 pin 1 (Wait States on page E for ZYMON EPROM or other firmware)

If pages C and D are vacant, or contain high speed memory, e.g. RAM, then make no more connections to assembly P5. Otherwise:

Connect P4 pin 3 to P5 pin 2 (Wait States on page D, for e.g. EPROM programmer, resident BASIC or other firmware.)

Connect P4 pin 4 to P5 pin 3 (Wait States on page C, for e.g. EPROM programmer, resident BASIC or other firmware.)

P6

P6

1
2
3

The connections on the P6 assembly select the polarity of the keyboard strobe.

Positive pulse or positive edge strobe

If the keyboard used has a strobe which is a positive pulse (a temporary transition from 0 to 1, and back again) when the data are valid, or if it has a strobe which exhibits a single transition from 0 to 1 when data are valid, then link positions 2 and 3 on assembly P6.

Note: This polarity strobe is the one which is preferred. If your keyboard can provide either polarity use a positive pulse or edge strobe. If your keyboard can provide only a negative pulse or edge for its strobe then use the following option on the LKP-1 card:

Negative pulse or negative edge strobe

If the keyboard used has a strobe which is a negative pulse (a temporary transition from 1 to 0, and back again) when the data are valid, or if it has a strobe which exhibits a single transition from 1 to 0 when data are valid, then link positions 1 and 2 on assembly P6.

Note: Only use this option if your keyboard is unable to provide the preferred positive pulse or positive edge strobe, since it makes your LKP-1 card "non-standard".

P7

P7

1
2
3

The link needed on this pin assembly will depend on an earlier option, as follows:

If U9 has been chosen to be a non-inverting buffer type 74LS244 (fitted to suit keyboard data which are non-inverted), i.e. the preferred arrangement, then link pins 1 and 2 on pin assembly P7.

If U9 is a inverting buffer type 74LS240 (fitted to suit keyboard data which are inverted), then link pins 2 and 3 on pin assembly P7.

P8

P8

1
2
3

This pin assembly provides an option to connect the wait signal output (NWAIT) to a different edge connector position if necessary to suit a different bus standard. The connection will depend on the bus standard in use:

ISBUS-A, ISBUS-B, Interak

These have the NWAIT signal on edge connector position A34. To suit these buses link pins 2 and 3 on pin assembly P8.

KBUS-5, KBUS-12

These have the NWAIT signal on edge connector position A30. To suit these buses link pins 1 and 2 on pin assembly P8, and connect edge connector A30 (there is a connection point provided near the edge connector) to the hole provided to the left of pin 1 of assembly P8, or indeed directly to pin 2 of assembly P8 if preferred, this latter suggestion rendering the link between pins 1 and 2 superfluous.

Other Buses

Proceed as indicated for KBUS-5 and KBUS-12 above, but instead of connection to edge connector position A30 connect to whatever edge connector position the bus in use specifies for the NWAIT signal.

Although it is obvious it is worth stressing that if no wait states are required from the wait state controller circuit on this card then

no connections are necessary on assembly P8. If a push fit link or connections to a switch are used on assembly P8 then the link or switch can be used to enable/disable wait states.

Variable Resistor RV1

This sets the number of wait states to be added for a given CPU clock frequency at chosen addresses. It normally has an effect only if one or more suitable connections have been made to pin assembly P5, as described earlier in this section of the Manual. Turning the operating screw fully anti-clockwise provides no wait states for accesses to the chosen addresses, gradually turning it clockwise provides progressively one, two, or more wait states for accesses to the chosen addresses. When commissioning a new system it is probably best to be safe and wire pin assembly P5 to suit all addresses where slow memory devices (e.g. firmware EPROMs) are located, and to turn the RV1 adjusting screw clockwise for three or four turns to ensure at least one wait state is provided for the selected addresses.

(Detailed setting up information is provided in Section 3.2 of this Manual.)

2.4 DETAILED CIRCUIT DESCRIPTION

The circuit diagrams towards the end of this Manual will be taken as the basis for the detailed circuit description. The purpose of this Manual sadly (for the reader, not the writer) does not extend to being a course on digital circuit design, and so it will have to be assumed that a certain amount of background knowledge is possessed by the reader.

Mostly, the components on the diagrams and in the parts list use the designation letters specified in ANSI standard Y32.2-1970. In a way these letters are fairly irrational (e.g. "J" is a connector, "Q" is a transistor, "U" an integrated circuit, and so on), however as it is a standard it has been adopted here. The component overlay diagram uses the same designations as for the circuit diagrams.

A block diagram is provided, which also serves as a "map" showing the user where he may find the particular section of the circuit in which he has an interest. Each of the sections represent a logical unit of the whole circuit. Particular care has been taken when preparing the diagrams to ensure, as far as is reasonably possible, that the logic flow begins at the top-left hand corner of the drawing, and continues downwards from left to right. Another convention which has been followed as rigorously as possible is to have the inputs to the left of each circuit block and the outputs to the right. Although this is a very logical and sensible approach to drawing circuit diagrams, it is surprising how often these ideas are disregarded.

In order to include the information which it is desired to present on the circuit diagrams (pin numbers, function names, power supply pins etc.), it has been necessary to use several sheets of paper. However great care has been taken in partitioning the diagram to turn this apparent disadvantage into a positive advantage, by breaking the circuit up into individual sub-functions which are more easy to understand a step at a time. Even the order of the various sheets has been given close attention, so that as far as possible the source of a signal is shown on an earlier diagram before it used on a later one. All signals which connect to a part of the circuit on a different page are given names, and their source or destination is shown in the form (e.g.) SIG1 3/10,12(4);6/9(5). This (ficticious) example means the signal called SIG1 is connected to U3 pins 10,12 on the circuit diagram sheet (4), and also U6 pin 9 on sheet 5 of the diagram.

So as not to interfere with the understanding of the logic flow, not all power supplies are shown on the integrated circuit drawings. Instead, each sheet of the diagram contains a table of the integrated circuits on that sheet, their type number, and their power supply connection pins. This does not apply to power supply connections which represent a logic level input, for example 0V for a logic "0", or +5V for a logic "1"; these are shown connected to the integrated circuit pins. An effort has been made to show all pins of each integrated circuit, even the ones which are not connected to anything else. Such pins are marked "N.C.", which means "not connected".

The Parts List is to be found at the very back of the Manual, for easy reference. It is organised in two ways; firstly by component reference number, which gives the component value if the reference number is known, and secondly by component value, which gives the reference numbers of all the components which have that value. The latter method is more convenient when checking a kit of parts and assembling the card; for example it is often useful to know where all of the components of a given value should be located if you finish construction and find one or two items left over. Later, you will want to know the value of a component of a given reference number, and the first method of forming the parts list will be more appropriate. To minimise the well known chore of searching all over a circuit board seeing if you can find say C11, or R17, which have become temporarily invisible, the components on the component overlay have been numbered in ascending numerical order, starting at the top left-hand corner and working across and down to the bottom right. (So if you are looking for an elusive R17, you will know you are getting warm if you see R16 or R18: R17 won't be far away.)

To help users carrying out tests on the card, or wishing to modify it, both ends of such components as resistors and non-polarised capacitors are identified on the circuit diagram; for example if it is wished to check the output pin 12 of open-collector gate U2 (on sheet 4 of the circuit diagram) it can be seen that it is connected to end 2 of R5, end 1 of R5 being connected to +5V.

On the component overlay diagram horizontally positioned components should be taken as having end 1 to the left and end 2 to the right, and vertically positioned components should be taken as having end one to the top of the diagram, and end 2 to the bottom. In an effort to help users all components have been placed on the card in a similar direction, so that for example all the I.C.s are the same way round, similarly the electrolytic capacitors and diodes.

Section 5 of this Manual also includes various timing diagrams, which may be an aid to understanding certain parts of the circuit.

As the circuit diagram has been drawn split up into logical blocks, these represent convenient sections into which the circuit description may be divided.

Sheet 1. The Block Diagram.

This shows the complete circuit in block form. In Sections 2.1 and 2.2 of this Manual general descriptions of the way the card works have been given and it is now time be more specific. The Block diagram is a little like the whole circuit diagram on one page, and is of course fairly comprehensive as a result. Once it has been studied it should be thought of as a "map" showing where to find the detailed diagram corresponding to each block, and to this end the appropriate sheet number of the circuit diagram is given beneath each block.

The Block Diagram shows quite effectively the two separate circuits which are present on the LKP-1 card. The first of these circuits is represented by the upper eight blocks of the diagram, and is the

keyboard interface itself. The second circuit is represented by the lower three blocks, and is the 4K page decoder and wait state controller circuit, which is entirely independent of the keyboard interface part. (It will be remembered that it is only here for the following main reasons: Firstly because users of early "Kemitron" systems who are upgrading to the Interak 1 system may still need a 4K page decoder while their changes are incomplete, secondly because there is a need for a wait state controller somewhere in the system, and thirdly there was a convenient amount of unused space on the LKP-1 card which meant the wait state controller could be added at very little overhead cost.)

As the lower three blocks represent the simpler circuit, the description will begin with these, in order to limber up for the description of the more complicated upper eight blocks.

The first of the three blocks is the 4K Page Decoder. The term "Page" is used here to indicate a contiguous block of memory starting on a 4K boundary, e.g. 0000H, 1000H, 2000H, . . . , F000H. There are 16 such pages in all and together they make up a 64K (16 x 4K = 64K) block of memory, sometimes called a "Chapter", or "Bank".

Any of these sixteen 4K Page decode signals can be used for the user's own purposes (mainly in very old systems which still use these page selects in their decoding). Up to three of the 4K Pages (or more if extra gates are added on the patch areas) can be connected directly via selection links to the second block, which represents a three input logic gate. The output of the gate triggers an adjustable monostable which drives the bus NWAIT (wait) line via a suitable on-board open collector driver, actually part of an already used gate pack in order to keep complexity to a minimum.

The selection links are usually chosen to correspond to an area of memory which contains relatively slow memory, such as EPROM based firmware. (Slow in this context being around 450 ns, i.e. about half a millionth of a second!) With the selection links so chosen, accesses to these areas will trigger the monostable to provide a pulse which will hold the NWAIT line low long enough to force the CPU in the system to prolong whatever transaction is being conducted on the bus (collecting the fares perhaps). The transaction can be prolonged sufficiently to suit the speed of memories in use. (With the usual 4 MHz Z80A CPU one wait state is sufficient to suit 450 ns access time memories.)

The main part of the circuit on the Block Diagram begins with the block at the top left-hand corner. This shows the address selection links or switches (whatever is preferred by the user). The second block (the 8-bit Port Address Decoder) receives two sets of inputs: the desired address, as set by the links or switches, and the lower eight bits of the system address bus. NIORQ (the I/O request signal from the Z80A-CPU) and NRDS (the read data strobe) are also brought into the address decoder to ensure that the LKP-1 card responds only to an I/O Port Read (Input) instruction from the CPU, i.e. it ignores any write (Output) instructions, and it does not respond to any addresses in the memory space.

There is therefore an output from the 8-bit Port Address Decoder when a read of the chosen port is in progress. This output is used as an input to the Read Synchronisation Flip-Flop, which will have previously been reset by the Power on Reset circuit block. The purpose of the Read Synchronisation Flip-Flop is to resolve any doubt should the CPU choose to read the LKP-1 port just after a key has been pressed and the data are still changing. The signal used to assist here is the lowest of the three inputs to the Read Synchronisation Flip-Flop, and is the strobe bit output from the 8-bit latch.

There are two outputs from the Read Synchronisation Flip-Flop. One is used to enable the Octal Data Bus Buffer so that the data (if any) stored in the 8-Bit Latch are transferred to the system data bus. If data are in the latch, which would have been indicated by the presence of a 1 as the strobe bit output, the other output from the Read Synchronisation Flip-Flop goes active (low) and clears all bits in the 8-bit latch. This only happens at the end of a successful read, after the data are safely on their way. If no data were in the latch then the strobe bit remains '0', and the Read Synchronisation Flip-Flop does not change state. If the data were just about reaching the latch then the strobe will be '0' turning to '1', and so it may or may not be recognised, and it is in this contingency that the Read Synchronisation Flip-Flop performs its most valient service. It ensures that if the strobe is recognised then so will be the data, and if it is not recognised the data (which may be suspect) will not be used until the next cycle, when they definately will be valid. The details of the circuit will be given later when this part of the circuit diagram is being discussed.

This concludes the description of the Block Diagram.

Sheet 2. Address Decoder

The LKP-1 Card is normally present in the I/O Port Space of the Z80A-CPU. There are 256 Ports in an Interak 1 System (and many other Z80A Systems), and therefore each one including the LKP-1 Port is uniquely identified by an eight-bit address (2^8=256). The eight bus address lines (AB0 to AB7) are compared with the eight selection switches or links. The switches must be set to the complement of the desired Port address. It is quite easy to remember this requirement since this results in the appropriate switch being ON for a ONE and OFF for a ZERO. The detailed switch settings have been discussed already, in Section 2.3 of this Manual.

The comparison is carried out by eight EX-OR open collector gates (U4 and U5) wire-OR-ed (EX-OR-ed?) together. End 2 of the pull-up resistor R4 goes high ('1') whenever the addresses match the address set as a complement on the eight switches or links, i.e for the one chosen Port. All 255 other Ports will not be recognised, because for any other Port but the chosen one at least one address line will not match the switch setting. The output of the mismatching EX-OR gate will go low pulling all the other matching ones down with it, as they are all wired together. (This does not cause any damage since open-collector gates can be connected in this way.)

As the I/O Port addresses are obtained from the same bus as the memory addresses the comparator so far described also responds to a read or write of a good many memory addresses, and could thus cause corruption of data on the data bus when the affected memory locations were read. The signals to prevent this are to be found as inputs to the 3-i/p NAND gate U2 shown on Sheet 2 of the circuit diagram. For output U2 pin 8 to go low all the inputs must be high. U2 pin 11 is high when NIOREQ is low, i.e only for an I/O request. U2 pin 10 is high only when NRDS is low, i.e. only for a read, and U2 pin 9 is high only as previously described, i.e. when the lower eight address lines bear an address which exactly matches the one specified by the switch settings. In short U2 pin 8 goes low only when the CPU in the system is executing a read (input) of the specified I/O Port. It will be high at all other times since the output of a NAND gate goes high if any one or more of its inputs are low; all inputs have to be high for a low on the output. The NAND gate signal NSEL is inverted to give also a signal SEL. NSEL goes low when the keyboard Port is selected for reading, and SEL goes high.

As well as performing the necessary inversion of the logic levels on the NIOREQ and NRDS bus input lines the U3 sections improve noise immunity as they are Schmitt trigger devices. U3 pins 11 and 10 are available for any special purpose or may remain unused, and U3 pins 9 and 8 is simply an inverter, its Schmitt trigger properties being immaterial here. R6 is a pull-up resistor which is required because U2 has been chosen as an open collector device (not because of its function here but because it will later be driving the open-collector NWAIT line of the bus).

Sheet 3. Data I/O, Control

The description of this sheet of the diagram will begin in the bottom left hand corner rather than at the logical top corner. J1 is the input from the ASCII encoded keyboard, which may draw its power from the +5V, 0V, and optionally -12V, rails shown to the left of the J1 connector on the drawing. There are seven bits (B0 to B6) plus a strobe (STB), usually pulled up by the eight pull-up resistors contained in SIL 1. The seven bits of data are latched in U8, and are conducted, through the buffer U9, onto the data bus lines DB0 to DB6 when the time is ripe. U9 is normally a non-inverting type, but a pin-compatible buffer can be substituted to accommodate a keyboard which can give only inverted data.

The strobe (J1 pin 8) can be inverted or not inverted, according to whether or not the inverter U3 pins 13, 12 is linked into the circuit on P6. Since the presence of the strobe signal edge indicates that valid ASCII data are available from the keyboard, the strobe is used to clock the data into the octal latch U8. The required clock polarity is a postive edge (0 to 1 transition). When the seven bits of ASCII data are clocked into latch U8 a "pseudo strobe" is clocked into the highest bit (input U8 pin 18, output U8 pin 9). The details will be engendered shortly but for now trace the route of the pseudo strobe from U8 pin 9 to U6a pin 12 and via either U6a pin 9 or 8 to U9 pin 2, and hence, at the appropriate moment, to the eighth data bus line DB7, where it is to be recognised by the operating software in the

remainder of the computer system. The software will normally follow the convention that when a read of the keyboard port results in data which have a '1' as their highest bit, the lower seven bits can be taken as containing valid ASCII data from the keyboard. The clever part of the LKP-1 latched keyboard port is that once a key has been pressed it will remain available for reading by the CPU until either it has actually been read or another key is pressed; it is no longer necessary to "poll" the keyboard constantly to ensure no keystrokes are lost.

The two flip-flops U6a and U6b are the "Read Synchronisation Flip-flops" which were referred to in the Block Diagram description. They ensure that the ASCII data which the CPU reads does not change except in synchronism with the read cycle of the CPU itself. Its operation is effected by careful manipulation of the timing of the "pseudo strobe" which is used to guarantee to the CPU that the ASCII data it is reading is valid. The timing diagram in section 5.3 of this Manual may assist further study of this part of the circuit, which is described next:

Begin at the top left hand corner of the Sheet 3 diagram (at last). When power is first applied C12 is discharged, and so holds the Schmitt trigger U10 input pin low, forcing its output pin 8 high irrespective of the state of the other input pin 10. U10 pins 12 and 11 act simply as an inverter (the Schmitt function being immaterial here and the other input pin 13 being permanently enabled by the direct connection to +5V.) Note that the direct connection is permissable because the inputs to U10, being an "LS" device, are Schottky diodes; had standard TTL with its multiple emitter input connection been used, a series resistor to +5V would have been necessary to provide protection against transient overvoltages causing reverse base emitter voltage breakdown of the TTL multiple emitter inputs.

As the signal has been inverted, the U10 output pin 11 is low at switch on and "sets" flip-flop U6b via the S input pin 4. As its Q output is thus '1' the opposite output pin 6 is '0', which clears all outputs of U8 to '0' also, under the action of the '0' on the Clear input U8 pin 1. The '0' output on U8 pin 9 is connected to U6b pin 1, the Reset input, which causes U6b output pin 6 to go to a '1', so removing the Clear signal at U8 pin 1. At this stage U8 is ready to receive data from the keyboard, although the rest of the circuit on the LKP-1 is still in the process of initialisation. U8 output pin 9 is '0' at the moment and thus presents a '0' to U6a input pin 12. U6a is neither Set nor Reset because the respective input pins 10 and 13 are both tied to +5V and so the U6b outputs are indeterminate. (The direct connection of the inputs to +5V is allowed since the specified "LS" device has Schottky diode inputs.)

During the time all the events described above have been taking place C12 has been steadily charging via R8 and R9. (It should perhaps have been mentioned earlier that the low value of resistance for R9 causes no hinderance to the logic '0' so far presented to U10 input pin 9. The purpose of R9 since it is so small, and CR1 because it is reverse biased will not be clear at this stage, but is explained

below.)

After a short while R8 charges C12 sufficiently to give a logic '1' at U10 input pin 9. If the NRST line connected to the other input pin 10 is also '1' (which it will be a short time after power is applied) then U10 pin 8 will go low and U10 pin 11 will go high. Although the transition from '0' to '1' at U10 pin 9 is very slow it is turned into a single reliable transition because of the Schmitt trigger action of U10. Thus U6b pin 4 is '1', which leaves U6b Reset (by the '0' on its Reset input).

If the power is removed it is necessary to discharge C12 quickly so that the above sequence of events can be repeated when power is restored. The discharge of C12 is accomplished by connecting it via R9 and CR1 to the +5V rail (which will rapidly fall to 0V). CR1 acts as a short circuit across R8 when power is removed and so hastens the discharge of C12. R9 limits the discharge current to about 25 mA maximum, and so a small signal diode can be used for CR1. C12 is specified as a miniature low leakage Aluminium electrolytic capacitor, and so would be able to tolerate much higher rates of discharge, however some users may be rich enough to afford a Tantalum type, although Tantalum construction confers no benefits in this circuit. In fact one of the serious weaknesses of Tantalum capacitors is their very poor tolerance to high rates of discharge and the limiting effect of R9 will ensure that no damage will be done to C12 even if a Tantalum type is substituted for that recommended.

Once C12 is charged the power on initialisation is complete. However as the NRST line from the bus is connected into the circuit, the same sequence of events will be entered whenever the Reset switch (if any) is operated on the CPU card. Pressing Reset on the CPU card will therefore clear any character which was latched on the LKP-1 card when power was first applied.

When the keyboard Port is read the SEL signal goes high, and the NSEL signal goes low, for the duration of the NRDS pulse. This read can be carried out either with or without keyboard data latched on the card. We shall first consider the case just after switch on or reset, before a key is pressed, and we will then go on to consider what happens if a key has been pressed on the keyboard.

Notice that the first of the two flip-flops is clocked on the leading edge of the SEL signal, and the second flip-flop is clocked on the trailing edge of NSEL, which also corresponds to the trailing edge of SEL.

If no key has been pressed U6b input pin 12 is '0', thus when U6a is clocked (by a CPU read of the Keyboard Port) U6a output pin 9 will be 0, since the output of a D-type flip-flop such as U6a follows the input when it is clocked. This '0' will be routed via the octal buffer U9 to data bus line DB7, and so when it is read very soon after, it will indicate "no valid Keyboard Data". U6a output pin 9 is also connected to U6b input pin 2, and when U6b is clocked at the end of the Keyboard Port read cycle, output pin 5 will be '0', and thus pin 6 will be '1', i.e the state of U6b will be unchanged.

Successive reads of the Keyboard Port will be exactly as described above, and the operating software will continue to see no valid data.

When a key is pressed on the keyboard, the data are latched into U8 and the '1' on U8 pin 18 (direct connection to +5V is O.K. as an "LS" device is used, which has Schottky diode inputs), and thus U8 output pin 9, the "pseudo strobe" will now go to a '1'.

The start of the next Keyboard Port read cycle will therefore result in output pin 9 becoming '1', since input pin 12 is '1', and this will be routed through buffer U9 to data bus line DB7, which causes the operating software to recognise "Valid Keyboard Data". After the data have been safely read, at the end of the cycle, the '1', which is now present at U6b input pin 2, will be clocked through to U6b output pin 5. Output pin 6 will therefore go to a '0' which will clear all eight outputs of U8 to '0', under the action of the U8 pin 1 Clear input. No matter how quickly the operating system software comes back and reads the port again, the same data will not be read a second time; the action of a successful read is to clear all the data including the strobe.

As the actions of the user pressing the keys on the keyboard, and the computer reading them, are entirely unsynchronised, special examination has to be made of the operation when a key is pressed at the worst possible time, e.g. when the keyboard data and strobe are changing just as they are being read. Without the special "Read Synchronisation" circuit on the LKP-1 card, this could cause a problem, since a read could be carried out of valid data which would be rejected if the strobe wasn't quite ready, but the action of reading the data would wipe them out altogether so they would be missed next time.

There is no problem of this nature on the LKP-1. U6a is clocked at the beginning of the cycle, before the data are needed, and U6b is clocked at the end, after the data are read. If the strobe just fails to get in at the beginning, the data will not be read, and will therefore not be cleared, and consequently will be read next time. If the strobe gets in just at the beginning then the data will certainly be valid; they will be read and the strobe cleared so that the data will not be read again.

The links on P7 can supply either polarity of strobe to the buffer, and the appropriate connection will depend on whether or not an inverting or non-inverting buffer has been fitted for U9 to suit a particular keyboard. Section 2.3 of this Manual summarises the various settings, and also includes instructions for the appropriate links to be made on P6.

Two of the Schmitt trigger NAND gates are unused. Their pin numbers are shown at the top of the diagram.

Sheet 4. 4K Page Select, Wait States

It will be remembered that this part of the circuit has nothing to do with the basic function of the LKP-1 card. It is simply using up some spare space in providing a circuit which is quite useful, but would not merit a whole card of its own, and as very early users may be replacing an old Kemitron "DCR-6" keyboard which had a 4K page decoder they will find their task easier if the same decoder is present on the alternative LKP-1 card.

U1 is a 4-line to 16-line decoder which has 16 possible different combinations of address input. Each of the outputs therefore represents one sixteenth of the total 64K memory space, i.e. 4K each (since 64K divided by 16 = 4K). The two enable inputs G1 and G2 are connected to the bus lines NMREQ and NRFSH (inverted) respectively. NMREQ is used because the 4K page decoder is desired to respond only to addresses in the memory space, and NRFSH (inverted) is used to ensure that whenever NFRSH is low G2 is high, which prevents any outputs from U1 while a refresh cycle is in progress. There are sixteen outputs PS0-PSF which correspond to the following addresses (suffix "H" means hexadecimal addresses below):

PS0	0000H-0FFFH
PS1	1000H-1FFFH
PS2	2000H-2FFFH
PS3	3000H-3FFFH
PS4	4000H-4FFFH
PS5	5000H-5FFFH
PS6	6000H-6FFFH
PS7	7000H-7FFFH
PS8	8000H-8FFFH
PS9	9000H-9FFFH
PSA	A000H-AFFFH
PSB	B000H-BFFFH
PSC	C000H-CFFFH
PSD	D000H-DFFFH
PSE	E000H-EFFFH
PSF	F000H-FFFFH

If the 4K selects are used in your system (e.g. early Kemitron) they can be taken from the appropriate outputs of U1, but they are more often used for another purpose:

One, two or three of these can be connected to the three inputs of NAND gate U2 pins 1, 13, 2. The physical layout of the board makes it easy to connect the three most likely candidates for use in an Interak 1 system; see Section 2.3 of this Manual for more discussion of this topic.

R1, R2, R3 ensure that any unused inputs are suitably terminated, but high enough value of resistance have been chosen so that there is no conflict when the input is driven low by an output from U1 or elswhere. As U2 is an open collector device R5 is used to pull its output high when necessary. The U2 output pin 12 goes high when any or all of its inputs go low, i.e. when the address bus bears a

selected non-refresh memory address. This positive edge triggers an adjustable monostable U5, which drives the NWAIT bus line low via the open collector driver U2 pins 5 and 6, wired as an inverter. The monostable pulse duration is varied by RV1 in series with R7, and sets the number of "wait" states. The values have been chosen to suit operation in an Interak 1 system. (More detailed setting up information is given in Section 3.2 of this Manual.)

R7 is used to ensure that RV1 can be reduced to zero ohms without taking the monostable total timing resistance below its minimum recommended value. For dedicated applications the expense of RV1 can be saved by omitting it and R7; fitting instead a predetermined single resistor R7a. Although half of U5 is unused, space has been allowed on the circuit board track to add a timing resistor and capacitor, so that any special needs for an extra monostable can be met more easily. If this second monostable is also used for wait state generation it can be connected to U2 pin 3 or 4 by cutting the existing connections to +5V. (The existing direct connections to +5V are permissable without the expected series resistor because U2 is an "LS" device with Schottky diode not multiple emitter inputs.)

The P8 link is normally made to bus pin A34, which carries the NWAIT signal in Interak systems, but alternative arrangements can easily be made to suit other standards, notably the "Kemitron" buses, KBUS-5 and KBUS-12.

Sheet 7. Key to Symbols, and Power Supplies

This sheet of the diagram is pretty well self-explanatory, but it will be explained nevertheless. It gives general information which is not often required but is handy for reference.

The table at the left of the diagram shows the various symbols and conventions which have been used on the earlier sheets of the circuit diagram.

To the right are the power supply connections. The LKP-1 itself only uses 0V and +5V; +12V is not used at all, and -12V is merely routed to the keyboard connector to suit any old-fashioned keyboards which still require -12V in addition to the usual +5V.

Below these are shown all the decoupling capacitors, which provide low impedance connections between the supply rails and 0V. Without them them there is a risk that the impedance of the power supply would be large enough to present a common load to the various logic elements on the card; when one element switched the voltage dropped in the common load could be sufficient to transfer the signal to some other logic element and cause switching which should not take place. The decoupling capacitors, particularly the electrolytic types also act as a reservoir of charge to supply the local power needs of the integrated circuits as they switch until the main power supply regulator in the system can respond to the demand.

The small value decoupling capacitors should be of a suitable type. In general all common types of ceramic construction are suitable, but

some care should be exercised when using plastic film types. For example polyester film is an acceptable dielectric but the capacitor should be of stacked dielectric construction rather than wound, since the latter method has so much inductance as to increase the total impedance at high frequencies not reduce it. If in doubt ask your supplier for decoupling grade polyester or ceramic capacitors.

This concludes the detailed circuit description.

3.1 CONSTRUCTIONAL NOTES

1. Read all documents very carefully before starting.

2. There are no Static Sensitive devices in the present kit of parts, so everything may be handled without special precautions. Identify all the components and using the Component Overlay, and the Parts List, work out where they all going to fit before soldering anything.

3. The top side of the board is the side which is visible when the card is viewed in the same way as is illustrated in the Component Overlay diagram, i.e. the diagram is drawn looking at the top side. The other side is the underside and the components are inserted from the top side and soldered on the underside, when the time comes.

4. Carry out any drilling or filing necessary to fit the card in the rack, and to bolt on the front panel. (This work should not be necessary, but if it was it would be a lot more difficult once the card had been assembled.) In order to get the longest life from the edge connector sockets in the rack it is a good idea to chamfer lightly all of the edges of the card around the gold-plated area - but do not overdo this!

5. Check that there are no obvious defects on the board, e.g. damaged or short-circuited track etc. Look especially beneath the IC socket positions since they will be hidden in the finished job.

6. Consult the Component Overlay, and the Parts List, to determine what goes where. Any convenient order may be followed, but a typical method is to start with the lowest height components and work up.

   The following steps can be used as a check-list:

   (a) Fit resistors R1-9, (Note! Fit the correct values - the colour code is given in the Parts List.) They may be fitted either way round.

   (b) Fit the diode CR1. (Note! Fit it the right way round - see the Layout Diagram and the sketch on the Parts List.)

   (c) Fit IC sockets U1-U10. Be sure to use an acceptable type of socket if you are going to take advantage of the board supplier's fault-finding service - see the Fault Finding Section of this Manual for further remarks on this subject. Make the identifying mark on the socket correspond to the Pin 1 end of the DIL switch or IC. Do not plug any components into their sockets yet.

   (d) Fit RV1.

(e) Fit C1-13. (Note! C12 and C13 are polarised types which must be fitted the correct way round. The "+" lead of the capacitor will be marked "+", or can be identified by a process of elimination as being the lead which is not marked "-".) Consult the sketches in the right-hand column of the Parts List (at the back of this Manual) for further guidance. Go through the whole list of capacitors, comparing the different types and quantities supplied, if you are not used to capacitor markings, until you are sure you know which is which.

(f) Fit the two 9-pin 0.1" socket strips which are used as sockets for SIL 1 and SIL 2. One type of socket-strip which may be supplied is just like half a dual in line (DIL) integrated circuit socket, and should be fitted in the same way as such a socket.

The other kind of socket strip comprises a number of formed sockets on one-piece carriers. Do not break off the carriers yet! Note that there are ten holes in the vicinity of SIL 1, and the socket strip for SIL 1 should be installed in the correct nine of these. Solder the strips in position and when you are sure everything is correct, and only when, break off the carriers by bending them gently back and forth with long nosed pliers, being certain not to distort the socket parts in any way.

(g) Fit the 0.1" pitch pin assemblies P1-P8 (these comprise six 3-pin and six 5-pin assemblies in various quantities and positions as indicated on the component overlay diagram, immediately before the parts list at the end of this Manual.) Some of P1-P8 are made up from single assemblies, others use several. Pass the short length of the pins thorough the card from the top and solder on the underside, like all the other components. (For very low-profile work they can be mounted upside down, i.e. the long ends through the card, and the surplus cut off after soldering.)

7. Install the DIL switch S1 if a DIL switch is to be used, and SIL 1 and 2. The DIL switch is to be fitted the same way round as the integrated circuits. (Note! SIL1 and SIL 2 must be fitted right way round; pin 1 of the SIL Resistor packs will be identified in some way.)

8. If you wish, use a suitable solvent to remove any flux deposits from the track side of the board. (Note! Some solvents also dissolve some types of plastic.) Also note that over-zealous use of flux-removing solvents can actually cause trouble, by washing impurities into connectors and IC sockets. You can give some protection by covering them with masking tape, but in many cases it is better to ignore this step altogether.

9. If a metal front panel is to be fitted (which is recommended) cut out the slot for the ribbon cable connector plug J1, according to the drawing provided in the Diagrams Section of this

Manual. (Note! Take care to avoid scratching the metal card front).

10. Fasten all of the front panel components (brackets, handle, J1) to the front panel.

11. Connect J1 to the appropriate places on the board, according to the details given in Section 2.3 of this Manual, which are repeated below:

P1 and P2

These are optional connection points for connecting a front panel 20-way ribbon cable connector, J1. There is space on the card for an alternative p.c.b. mounting connector which can be used instead if no front panel is to be fitted. In either case P1 and P2 make useful test points. If they have been installed neatly a 20-way ribbon cable connector can be pushed onto them; this iis very useful for test purposes if a card has to be tested when the customer has used a non-standard connector.

The recommended connections for the front panel type of connector are exactly the same as would be made naturally if the p.c.b. type of connector was used; they are indicated diagramatically on sheet 3 of the Circuit Diagram in Section 5.4. The connections are also presented below for the convenience of the reader:

Pin Assemblies P1 and P2

	P1	P2	
N.C.	1	1	B0
N.C.	2	2	B1
N.C.	3	3	B2
N.C.	4	4	B3
N.C.	5	5	B4
N.C.	6	6	B5
Strobe STB	7	7	B6
-12V	8	8	(B7)
+5V	9	9	+5V
0V, Earth	10	10	0V, Earth

The above pin assembly identifications translate to the ribbon cable connections given on the next page:

Ribbon Cable Connector Viewed From Rear (Inside) of Front Panel

top

	B0	19	20	N.C.
	B1	17	18	N.C.
	B2	15	16	N.C.
	B3	13	14	N.C.
"P" indicates	B4	P 11	12	N.C.
polarisation	B5	P 9	10	N.C.
slot position	B6	7	8	Strobe STB
	(B7)	5	6	-12V
	+5V	3	4	+5V
	0V, Earth	1	2	0V, Earth

Ribbon Cable Connector Viewed From Front (Outside) of Front Panel

top

N.C.	20	19	B0	
N.C.	18	17	B1	
N.C.	16	15	B2	
N.C.	14	13	B3	
N.C.	12	11 P	B4	"P" indicates
N.C.	10	9 P	B5	polarisation
Strobe STB	8	7	B6	slot position
-12V	6	5	(B7)	
+5V	4	3	+5V	
0V, Earth	2	1	0V, Earth	

Note 1. No connection should normally be made to pins 5, 10, 12, 14, 16, 18, and 20 of the ribbon cable.

Note 2. Some keyboards provide more than 7 bits of data, and for example have a parity signal, shown as (B7) above, on their eighth output line. It should be ignored as the strobe signal STB is required on the eighth data line in an Interak system.

Note 3. Some keyboard manufacturers number their data output lines as B1 to B8, instead of the numbering shown above (B0 to B7).

Note 4. Some cable ribbon connector manufacturers allocate the numbers for the ribbon cable as 20 to 1 instead of 1 to 20. If in doubt use the polarising slot to establish the correct numbering (it is on the same side of the connector as the odd-numbered pins). Note also that the coloured stripe often found on grey ribbon cable is usually the pin 1 cable identifier.

Wire-wrapping is a recommended method of connecting the ribbon cable plug to the LKP-1 card. Another method is to use special

push on crimped connectors, or even, if you have no alternative, soldered connections directly to the pin assemblies.

12. There are various links to be made on pin assemblies P3 to P8 but as they may be different for different users, precise guidance will be deferred until section 3.2 next (Testing and Setting up).

13. If desired the board may be laquered on the underside. A suitable printed circuit board laquer should be used, and similar precautions should be taken as described in the earlier paragraph (no. 8), to prevent the connectors and IC sockets from becoming contaminated. It is probably safest to ignore this step if you are in any doubt, as a lot of damage can be done through lack of experience here. (Note! be sure not to laquer the gold-plated edge connector on the card, and mask the pin assemblies as well.)

This concludes the constructional notes. The next section of the Manual covers setting up and testing.

3.2 SETTING UP AND TESTING

1. Check that all components fitted so far are in the correct place, and have the correct polarity where appropriate. Re-read the constructional notes - important points are preceded by the loud word "Note!", and can be checked again now.

2. Inspect the board for dry joints, solder bridges and solder splashes, paying particular attention to areas where tracks run between IC pins. Shine a strong light through the board, and use a magnifying glass if you have one.

3. Apply power to the board and check the +5V supply at all the IC positions where this voltage is used, i.e. the corner pins of the ICs. If you consider you are likely to cause damage by carrying out this test, or are very confident of your workmanship then omit this step at your own discretion.

4. Remove the power, and wait for the capacitors to discharge (if necessary use a few hundred ohm resistor to discharge them more quickly), and insert all ICs the correct way round.

   Usually the ICs are supplied with their leads slightly "splayed" - don't just shove them into their sockets; use the greatest care. An IC insertion tool will hold the leads parallel at the right spacing; if you don't have such a tool, bend the leads slightly at their "shoulder", on a flat surface. The sockets supplied in complete kits have been specially selected for their ability to provide high reliability connections, but the foregoing warnings are intensified if you are using your own sockets instead. There are some remarks in the Fault-finding Section later on the subject of difficulties which have been met with certain types of IC sockets, so study this before proceeding if you are in any doubt.

5. Important! Re-check the orientation and position of all ICs, as an error can have disastrous consequences. As it is hard to check your own work, preferably get someone else to check it for you.

6. Make the appropriate links on pin assemblies P3 to P8. Refer to Section 2.3 of this Manual for details. If you are not sure about certain points, e.g. whether or not your keyboard has a positive or negative strobe then ask your supplier for guidance. If this is not convenient then make a guess; any minor faults which occur due to a wrong guess can be rectified at the Fault Finding stage later.

7. Set S1 (or the links which replace it) to a suitable Port address for the software in your system. If this is Interak 1 running ZYMON 2 the appropriate port will be 40H. Discussion of the port addressing has already been conducted in Section 2.3 of this Manual.

8. If you have any suitable contact lubricant (e.g. the "Evolube" proprietary product) apply a small quantity to the gold plated edge connector. This will greatly reduce wear on the gold plating and the bus sockets and will thus extend their useful life considerably. An alternative type of lubricant which has been used with no apparent ill effects is a branded product "Rocket WD-40"; however as it has extremely penetrating properties it should be used most sparingly to reduce the very real risk of lifting the gold-plated copper tracks which would render the card useless. Fit the card in such a position that you can adjust RV1 without removing the card, (or use an Interak extender card, which can be purchased from your Interak supplier).

9. It has to be assumed at this stage that you have a working system with fully tested cards, but of course if this card is the only Keyboard Interface card you have this will obviously not be the case. In such circumstances you will have to bring the system up to correct operation as best you can, perhaps seeking advice and reassurance from the card supplier, or perhaps "Interaktion", the users group for the Interak computer. There will usually be no difficulty in finding volunteers to test your card for you, but if you are a typical user you wouldn't dream of letting someone else have the excitement of trying out the card for the first time, so you will have to proceed as intelligently and cautiously as you can in the circumstances.

10. Connect everything appropriately (have one final check that you have wired it correctly first, particularly the power supplies, so as not to damage the keyboard). Switch the system on and hope that you receive your first message from the computer. (In the case of ZYMON 2 this will be a clear screen and the title near the bottom "ZYMON 2", its version number, and an invitation to "ENTER COMMAND".)

11. It may be that no picture is displayed at all. If so then perhaps the VDU card would be the first to investigate; leave the LKP1 card for the time being, but before you do try the system again without the LKP1 fitted, to make sure that it is not causing any disasters on the bus. If anything untoward is noticed (such as sizzling noises, or dense black smoke - no laughing matter) then switch off immediately and refer to the Fault Finding Section. Otherwise leave the power on and check carefully (by hand) for any over-heating chips, which needless to say is a bad sign; if they feel fairly cool try try some further procedures:

12. With the keyboard connected, hold the shift key down and type some letters, e.g. A, B, C, etc. If ZYMON 2 is in use these letters should appear in sequence across the bottom line of the screen, other software may behave differently. Once the bottom line is full press the reset button on the CPU card, and continue with the tests. With the shift key released try the same tests and verify that the lower case letters are displayed, i.e. a, b, c, etc. (Of course for this test the keyboard used has to be capable of generating the required codes, and the VDU has to be

capable of displaying them. For example the early "Kemitron" VDU-A, B, G, 3-card set shows totally unrelated characters when the ASCII codes for lower case letters are written to it; the VDU-K fitted with the standard ASCII character generator shows lower case letters correctly.)

13. Proceed to try all the keys, e.g. !, ", #, $, %, etc. and any dedicated control code keys on your keyboard, e.g. carriage return, backspace, and so on. Finally, using the control key on the keyboard, try all the control codes which your computer can recognise, e.g. CTRL-C (i.e. the control key held down while the letter C is pressed). This is used to re-boot the CP/M disk operating system, if you have disks, and it performs a related but far more humble function in the ZYMON and ZYBASIC programs. If anything untoward is noticed then you can look in the next section of this Manual ("Fault Finding") for some things to try.

14. Once the basic functional tests above are carried out try the keyboard again more critically. Make sure that the computer never receives a character when no key is pressed. Make sure that it always receives one character, and only one character, each time a key is pressed, and make sure the character it receives is the one that was pressed - don't accept the occasional % in a word such as th%s for example!

    The requirements mentioned immediately above can always be met by the LKP-1 interface when it is used with a good quality keyboard and a suitable cable, but of course the LKP-1 cannot do anything but transmit defective data produced by a cheap keyboard. As a rough guide, keyboards costing less than say fifty pounds will be prone to producing double characters if the keys are not hit cleanly, or will occasionally miss characters as the switch contacts wear and become contaminated, but a keyboard costing more than say eighty pounds should be totally immune from such faults for many years of hard use. Needless to say many users will be entirely satisfied with a cheaper keyboard; as with musical instruments you often need to be a virtuoso performer to be able to appreciate the subtle difference which results from the use of top-class equipment.

15. The 4K page select decoder and wait state monostable will obviously only need to be set up if this part of the circuit is in use.

    If no equipment is available then one wait state can be added to accesses of the chosen 4K pages by turning the RV1 adjustment screw fully anti-clockwise, and then clockwise typically two full turns.

    If it is desired to commission a system urgently, and no test equipment is available, it is permissable simply to turn the adjustment screw of RV1 fully clockwise, which adds the maximum number of wait states (typically about three or four). This will slow down the operation of the system, but will at least ensure that there will be no problem on accesses of slow memory due to

the absence of the necessary wait states.

16. If a dual trace oscilloscope, or some other suitable equipment is available, the wait state monostable can be adjusted more scientifically. An "extender" card which enables other cards to be operated outside the computer rack is available, and will make it easier to carry out the following procdure:

(i) Connect one channel of the oscilloscope to the NWDS line on the bus, i.e side A, line 3. Trigger the 'scope from say the falling edge of the signal on this line, when running the program given below.

(ii) Connect the other channel of the oscilloscope to the NWAIT line on the bus, i.e. side A, line 34 in most systems (ISBUS, Interak), but side A, line 30 on the less common KBUS-5 and KBUS-12 systems.

(iii) Turn the adjusting screw of RV1 clockwise a few turns, starting from the fully anticlockwise position. This is to ensure that at least one wait state will be present so as to guarantee that the computer will work.

(iv) Enter and run the following short machine code program. Although it is shown starting at 1000H it may be entered and run at any other convenient location since it has been written to be relocatable. The program is designed to set up wait states which have been selected in hardware on 4K Page "E", but if any other page is to be used instead then the byte E0H in the program below will have to be changed. (Note this is all only for Z80A use.)

```
1000  3200E0   START: LD (E000),A  ; access the chosen page by
                                   ; writing the contents of
                                   ; register A to it
1003  18FB            JR START     ; ... for ever and ever.
```

(v) With the above program running, adjust the oscilloscope so that it is triggering reliably on the NWDS signal, and select a timebase which displays NWDS to the right of the oscilloscope screen. Turn the adjusting screw of RV1 fully anticlockwise and observe that NWAIT has been driven low for a short period just before NWDS goes low . Under these conditions NWAIT is not low long enough to cause a wait state. (Since the program which is running is in high speed RAM, the lack of wait states on page "E" is immaterial to correct operation at the moment.) Do not be concerned at the poor quality of the waveform on the NWAIT line; it is an open-collector bus line being pulled up by a resistor of value 1k on the CPU card, and at the speeds involved the 1k can only do this relatively slowly.

Gradually turn the adjustment screw of RV1 clockwise. Observe that the duration of the pulse on the NWAIT line increases evenly as the screw is turned, and at a particular point the duration of the NWDS pulse, which has been constant so far, increases

abruptly. This is the addition of one wait state. Continue turning and observe the addition of more wait states as the RV1 screw is advanced still further.

Finally, leave the adjustment screw set to the appropriate position: Normally the slowest memory to be considered nowadays is 450ns, and only one wait state need be added to run programs contained in memories of this speed. Slower memories would require more wait states, faster ones would probably not require any wait states at all. As RV1 is continously variable it should be left midway between the position which adds one wait state, and that which adds two, i.e. in a manner of speaking the correct setting is "1.5" wait states.

17. As modern memory devices often exceed their stated specifications it is possible for an individual to "fine tune" his system if he wishes, to make it work as fast as it possibly can. This is done by removing wait states from as many pages as possible, and/or reducing the setting on RV1. (It seems invariably that no wait states are required in practice for the CPU on-board Boot EPROM, since it is on the CPU side of the buffers on the CPU card, and so does not suffer the delays through the buffers.)

    It is strongly recommended however that the computer is set up so that the memories are being accessed within their specified access time since any benefits due to small speed savings will be totally cancelled if they are made at the expense of potential unreliability of the computer system.

This concludes testing and setting up. The next section of the Manual covers fault finding, and return for service.

3.3 FAULT FINDING, RETURN FOR SERVICE

As a fault will be the result of any one or more of hundreds of possible things going wrong (he said cheerfully) it is of course not practicable to give any more than a guide to the location and correction of faults, but the procedures below will at least give some idea of how an attempt at fault-finding can be made.

Experience with other cards has shown that the major cause of faults in cards assembled from kits is due to soldering errors (e.g. "dry" or unsoldered joints, and bridged tracks). The next most likely cause is the setting up of the DIL switch address, then comes misplaced components and even obvious mistakes like missing ICs or ones plugged in upside-down. In the case of "bare boards", other common causes of faults are incorrect component substitutions (the user can't see any reason why he can't use some other component to that specified, but the LKP-1 card can!), and mis-insertion of i.c.s into their sockets; we shall have a great deal more to say on this subject later.

It is very rare for an IC to be supplied faulty (each one has to be tested and characterised by the manufacturer as part of the manuacturing process), and this is borne out by the fact that "ready made" Interak Cards never suffer defective chips; faults found on test are invariably due to some other cause.

However, all the time a board is being tested it is "at risk" (ICs are being pulled in and out, voltmeter and test probes are being prodded about and may short pins of ICs and pcb tracks together). It is frighteningly true that if you test a good board often enough you will eventually cause a fault!

When reading the following procedures remember that they are only suggestions, and there are plenty of other faults which often cause misleading symptoms.

If an oscilloscope is available some sinals can be observed on the LKP-1 card if is suspected this is at fault. Some places to look are given later in this section.

Many professional users will be in a position to find any faults without undue difficulty, and will therefore want to do their own fault-finding should the need arise. Other less experienced users will wish to do the same, but this time on the grounds that there is no better method of gaining a real understanding of computer hardware than tracing faults and fixing them themselves.

However laudable as these two aims may be, the company who supplied the kit will be prepared to help any of their customers who are in difficulties. The charge will probably be very little more than the cost of return postage and any parts which have been damaged.

There is no shame in admitting defeat - some tricky faults can baffle even the most experienced expert, and in many cases advanced test equipment will be needed which will just not be available to the average user.

If it is necessary to send a circuit board through the post, make sure the recipient knows to expect it. When making arrangements for the return of a board, be ready to quote the number of the invoice on which it was supplied, or approximate date of purchase. (A supplier will understandably not be so keen to help if the kit was purchased from someone else!).

For transit through the post, pack the board(s) well, wrapped in e.g. aluminium cooking foil for any which require anti-static protection (the LKP-1 doesn't), and remember to include your name and address, and arrangement for payment e.g. by means of an ACCESS or VISA card. A suitable postal service should be used both ways, e.g. Registered Post, Recorded Delivery, or Compensation Fee Parcel Post, even though this does cost more.

Warning.

There is a great art to replacing components and working in general on a plated-through hole board, and high quality, expensive special tools are needed, plus the skill and experience of people who have spent many long years learning their craft.

Having seen the results of some peoples' efforts we urge you to do anything other than try to unsolder an IC socket from a through-hole plated card. Cut tracks, plug the IC in with one lead bent out of the socket, and wire-wrap the missing connection onto the leg of the IC, anything! If you do have to remove a socket then don't try to salvage it. Smash it to pieces, and using tweezers remove the pins one by one, applying the minimum of heat and force to avoid pulling them out complete with the plated through holes. (The possibility of this activity being enjoined explains why it is not recommended that the very expensive turned pin in solid plastic type of socket be used. If the socket cannot be broken into pieces for removal then there is a severe risk of damage to the card when trying to desolder all leads of the IC at once.)

The same goes for discrete components. To remove a resistor, chop it in two; a new one is only a few pence and it will cost several hundred times that figure to buy a replacement for a damaged board.

Some General Fault-finding Procedures

The great difficulty in suggesting fault-finding procedures, is that the methods vary so much according to what equipment you have and your skill, knowledge and experience.

In the event of any trouble do switch off and re-examine the card, checking quickly for any overheating. If an integrated circuit is inserted wrong way up it will often cause a heavy burden on the power supply (which fortunately is well protected internally if it is one of

the recommended switch-mode types, and so should not suffer any damage). If the load is so great that it lowers the voltage on any of the supply rails then this could easily stop the computer working. It is almost certain that the heavy currents would cause the integrated circuit to overheat, in an extreme case causing smoke to come from it, and perhaps a minor explosion. Incredibly, integrated circuits subjected to such abuse can often still be fully functional when they are re-inserted correctly, but you are advised to replace them as soon as you can, rather than leave a potential source of weakness in the computer.

Experience shows that there is quite a good chance that there will be some visible physical fault, e.g. solder splashes on the tracks, unsoldered or "dry" joints, incorrectly inserted ICs, and so on, (e.g. ICs in the wrong sockets, or inserted badly, so that a pin is bent and makes a poor contact).

The integrated circuit sockets used in the kits are a high reliability type which has been most carefully selected after considerable experience. They have a tenacious grip on the ICs; also it is easy to enter the IC leads into the type of socket supplied, because of the lead-in ramp, and the generous and visible contact area.

Bare board users who have used some of the inferior types of socket widely available, must take special care to insert the ICs correctly, and should remember that poor sockets can be a regular cause of faults. (The "inferior" type of socket has a very flimsy contact which takes a weak grip on the IC leads, and has the contacts hidden behind small "windows" through which the IC leads must pass. It is vital with such a socket to ensure that the IC is inserted with the leads true and straight, so that they do not slip to the wrong side of the contact, or bend the contacts out of line - an IC insertion tool should really be used.)

Fault Finding Techniques

The main requirement in successful fault finding is a thorough knowledge of the whole card and the way it operates. Once you have this (and it is hoped you will have if you have studied this Manual so far) you will be able to localise the fault to a particular area of the circuit, and then "home in" on the particular source of the trouble.

There are two fundamental classes of fault which can be considered on the LKP-1 card. A reasonable name for them is "Active" and "Passive" faults. An "Active" fault in the LKP-1 card causes other parts of the system to stop working, whereas a "Passive" fault leaves the rest of the computer working but the LKP-1 itself does not produce the desired results. Due to the modular nature of the Interak computer it is quite easy to distinguish between these two classes of fault, simply by trying the computer both with and without the LKP-1 card installed.

Without a keyboard interface there is not a lot that the computer can do. Precisely what a computer does in the absence of a keyboard interface depends entirely on the operating software, but in the case of Interak 1 running ZYMON 2, many actions should all have taken place. (There is a very remote chance that at a 4 MHz clock frequency the access time of the EPROM containing ZYMON 2 may be too long for it to work properly, without the wait states provided by the LKP-1 card. However, ZYMON 2's first action is to copy itself down into RAM, and therefore very little code is actually executed in the EPROM. It is the execution not the copying of the program which puts the most stringent demands on the access time, so the chance of ZYMON 2 not working due to the absence of wait states is so remote as to be discounted).

If an Interak 1 computer comprising a CPU card, with ZYMON 2 installed, a VDU-K interface, and sufficient RAM, has been switched on without a keyboard interface, the following things should have happened internally:

The contents of the ZYMON 2 EPROM should have been copied down into RAM starting at 0000H, and execution transferred to the copy in RAM. This action is invisible to the operator, but its correct conclusion can be deduced by intelligent investigation of the power on jump flip-flop control on the CPU card, and the flurry of activity on the ZYMON source page as the code is being transferred to page 0 for execution.

The VDU screen is then cleared and the ZYMON 2 V.XXXX, ENTER COMMAND message is written on the lower part of the screen. The program then settles into a loop continually polling Port number 40H, the keyboard port, awaiting some input from the keyboard.

All this should happen without the LKP-1 card being plugged in; if it does not there is something wrong with one or other of the cards in the system. As very general rules, which should not be taken too literally, the following symptoms tend to hint at the following troubles:

A random unchanging VDU screen display:- CPU card not operating, CPU address links for power on jump on boot EPROM addressing wrong, or corrupted by some fault, or of course some VDU fault.

A repetitive geometrical pattern of data on the VDU screen: e.g. vertical columns of say "99", (or for a good doctor's diagnosis "say 99"):- a functional CPU card and VDU, but the CPU "out of control"; perhaps corruption of addresses or data, or absence of working RAM at the correct location.

As this Manual is the one which describes the LKP-1 card, it will have to be assumed that the other cards in the system are working (see their Manuals if they're not), and therefore the correct sign on message can be seen.

Switch off the computer, and install the LKP-1 card. This should not affect the results obtained so far. There may still be a fault on the LKP-1 card, but if it leaves the rest of the computer operational the

fault can be described as "Passive". If on the other hand adding the LKP-1 card "crashes" the computer then the fault is "Active".

In the latter case, remove the LKP-1 card and systematically remove all the chips which are connected to the edge connector, testing again at intervals to see if its behaviour is the same. The sort of fault on the LKP-1 card which would prevent the rest of the computer working is one which causes the LKP-1 to corrupt signals which are already present on the bus, by adding undesired signals of its own. Certainly the driver to the wait line should not be holding the wait line permanently low, since this would prevent the CPU from operating. If due to some fault on the LKP-1 card its data bus buffer was enabled permanently , or at intervals at the wrong time, this could adversely affect correct data on the bus, and so prevent operation proceeding as before. Possible candidates for such faults are something wrong with the port address decoding; for example if the LKP-1 card responded to more ports than just the single chosen port, or if it responded to addresses in the Memory space as well as the I/O space, this could explain the symptoms. (Just one or two open or short circuit connections would be sufficient to cause malfunctions of this kind.)

If the LKP-1 still causes trouble with all the ICs removed then this points to a physical wiring fault on the card, or the way it fits into the edge connector socket. Obviously a splash of solder across a couple of address, data, or control lines would be quite sufficient to prevent from working any computer into which the card was plugged.

In some ways a passive fault can be approached more logically. Scientific tests can be carried out with the power applied, and some signals and measurements can be made to confirm or deny possible explanations of the noted fault.

Keyboard Related Faults

Because the LKP-1 can be used with almost any parallel ASCII keyboard there are a fair number of options which can be wrongly selected, and which may explain possible trouble. If pressing keys does give results but they are not as expected there is a fair chance that the trouble may lie in the interpretation the user has put on the instructions to apply the various options, described in earlier sections of this Manual.

Great care must be taken with the provision of power to the keyboard. The -12V rail in particular if misapplied has the "potential" to do great damage.

Often keyboard manufacturers do not give very much guidance as to the signals their keyboards produce, and this is one major cause of difficulty. In the absence of such information, the LKP-1 user has to make some outright guesses as to which of the available keyboard signals he should use, which sort of strobe, and so on.

If only some keys appear to work on the keyboard and others seem completely "dead" this could be an indication that the lines are scrambled somewhere, for example one of the keyboard data lines has

inadvertently been used as the strobe. If this was the case then only keys which activated that particular line would have any effect on the computer.

Alternatively, if the majority of keys produce a response when they are pressed but the computer receives the wrong data, then there is a reasonable chance that the keyboard strobe is present. One expanation of this fault could be too large or too small a set of pull up resistors on the keyboard input data lines, or the keyboard strobe being set to work on the wrong polarity edge. Also the use of the wrong type of data bus buffer (inverting instead of non-inverting, or vice-versa), would be a simple recipe to make a malfunctioning computer keyboard interface.

If the fault is not related to the keyboard, then it is now most likely to be somewhere on the LKP-1 card itself.

Description of Circuit from the Point of View of Fault Finding

The circuit has already been described at length, in various degrees of detail in Section 2 of this Manual, but it is proposed to take another pass through the diagrams, this time from the point of view of looking for various things which can be considered when fault finding.

Sheet 1. The Block Diagram

With the exception of printing mistakes there is not much to go wrong here, but it is recommended that this be studied first when fault finding so that a "battle plan" can be formulated. Ask yourself where could the fault be to explain the symptoms you are suffering. For example if you are getting wrong characters when you press the some keys on the keyboard, and correct ones on others, could it be the port address decoder at fault? Not really - if that wasn't working there wouldn't be a response to any keys. Could it be the data bus buffer control lines? Again, not really, if it was being incorrectly driven it would have the same effect on all keys, it wouldn't matter which particular one was being pressed. By asking questions like this it should be possible to deduce from the block diagram alone, the general area of the fault, and you then move on to study the chosen part of the circuit in depth. (In the above example there is a possibility that the fault could lie on the individual data line paths, since the precise pattern of data does alter as different keys are pressed.)

Sheet 2. Port Address Comparator and Control Logic

This is fairly easy to test in a system which is working except for the LKP-1 card, since a useful test program is intrinsically built into the normal operation of the ZYMON 2 monitor program. After initialisation ZYMON 2 continually reads port 40H (the keyboard port in an Interak 1 system) waiting for a key to be pressed. The output pin 8 of U2 as explained in Section 2 of this Manual goes low when, and only when, the CPU is executing an input (read) instruction of the selected Keyboard I/O Port. The output of the gate is a convenient signal to use to trigger the oscilloscope. You will be very lucky to

have discovered the fault already, but you will be very close to it if you find there is not be a correct output; in that case check to see if all of the inputs do go high at least sometimes. Trigger the oscilloscope from one of the signals which seems O.K., e.g. the NIORQ line, and trace through the other gates until the fault is exposed. As the program is running in a loop the various states of the pairs of inputs to the eight EX-OR gates can be examined to see if they are exactly opposite in every case, which is needed to permit all the outputs to go high. The two output signals from the circuit on this diagram are NSEL and SEL.

Are you doing something silly, like setting the switches on when they should be off and vice versa? Are you setting them back to front, i.e. most significant digit confused with least significant? Is SIL2 plugged in right way round, are you sure pin 1 is pin 1? If the outputs of the gates are low when they should be high check that the pull up resistors are present and correct. Try removing the driving chip to the pull up resistors, to ensure the outputs really could go high given a chance.

Any small error in the construction of a computer will throw the whole logic out, and without a certain amount of experience and/or sophisticated equipment it is often only a matter of luck to be able to find a fault. To give luck a chance, you can probe the various elements of the circuit - although the various waveforms encountered generally will be meaningless, you can look for lines which are "stuck" at "0" or "1", or which don't appear to be reaching a low enough "0", or a high enough "1", inverters which don't seem to be inverting, and so on.

It may be helpful to read through the Detailed Circuit Description earlier in this Manual, and to study the Timing Diagrams both on paper and physically on the Card. As you gain an understanding of how the circuit operates you will be able to direct your own test procedures so as to find which piece of the circuit is malfunctioning, which is the first step to repairing it.

It is stressed again that if you do not have success in finding a fault that is present, you can always hand it over to someone else. The after sales service which is available to purchasers of the kits is one of the many things which mark out the Interak 1 System as being a unique and worth-while product.

Sheet 3. Data Output, Control

The easiest part of this circuit is the power on reset control shown towards the top left of the diagram. Once the capacitor (C12) has charged, taking less than a second. all the logic levels are static. To test the circuit earth end 2 of R9 momentarily to restart the power on sequence, (R9 being in series to limit the discharge current through C12 when this is done).

Check all the outputs of U8 are "0" after a power on reset, also the two "D" inputs and two "Q" outputs of U6 are also "0". Check that pressing a key on the keyboard causes a strobe to U8 pin 11, and a

change in the appropriate outputs of U8, especially output pin 9 which should go to "1" for an instant when a key is pressed. The "1" should also pass through U6a, and U6b, and the "0"s from the complementary outputs should also be present for the same brief interval; the U6b pin 6 output being used to clear U8 and restore the idling conditions until another key is pressed.

If there is some serious trouble on the data bus buffer U9, the operation of the circuit can be observed in slower motion by removing U8 from its socket, and replacing it with pin 1 bent out. It should float high, or can be connected to +5V to ensure that it does, and this will prevent the reading of data from the LKP-1 keyboard port from continually clearing U8. Whatever key is pressed on the keyboard will be latched in U8 until a new key is pressed, and the progress of the data through the octal buffer U9 can be observed at leisure (still triggering the oscilloscope from the NSEL signal).

The choice of links on P6 and P7 can be reviewed in the light of the signals actually found present on these pins, and the choice of a non-inverting or inverting octal buffer for U9 confirmed as being correct or otherwise.

(It may be useful to refer to a table of ASCII codes when checking the outputs from the keyboard; a table of these codes is given as Appendix 1 in Section 4 of this Manual.)

When measuring the very short duration pulses which occur when a successful read of the keyboard data is completed, remember they will not be visible on an oscilloscope unless it is carefully adjusted in the appropriate way to observe short pulses, repeated at random intervals. There are bound to be a few text-books on this subject in many libraries.

Page 4. 4K Page Select, Wait States

As mentioned at numerous intervals throughout this Manual, this part of the circuit has no logical connection with the rest of the LKP-1 card circuit.

To test it, it is suggested that the test program given in Section 3.2 of this Manual be entered and run, using of course a 4K page which has been wired in for wait states.

Connect the oscilloscope as described in Section 3.2 and ensure that the correct signals are produced. Fault finding here is quite straight-forward; if there is no NWAIT line output from U2b pin 6, see if there is an input (check U2 pins 3 and 4 are "1"). If there is no input to U2, i.e. no output from U5, then check for an input at U5 pin 10, and so on back through the U2a and U1. If the fault is traced to a particular IC check all the components around, and also that the pins obey the truth table or logic function for that device (a TTL data book is a great help here), and prise the IC out and check the pins again in the socket to make sure the lines are not jammed by short circuits and the like.

Always do this fault finding on the pins of the ICs themselves; this is because it is more likely to find a faulty socket connection than a faulty IC, especially if the unacceptable types described earlier in this Manual have been used.

Sheet 5. Key to Symbols, and Power Supplies.

There is not much on this sheet to go wrong, and it is a bit late in the day now to be checking if the power is connected, but if you have the world's most classic fault, a short circuited supply rail, then you will have to look at at all of the various decoupling capacitors shown on this diagram to see if they've got anything to do with it. Probably it is best to pull out all of the ICs just to be sure, but then it is a matter of cutting tracks, drilling out plated through holes and so on until you can find the faulty section of track. Better still send it back to the firm who supplied it, they were daft enough to volunteer to fix any fault you can put into a board, call their bluff!

This concludes the section on fault finding, so the authors of this Manual hope the card is fixed by now, because they've run out of ideas!

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4.2 APPENDIX 2: WAIT STATE GENERATION.

The subject of wait state generation has been covered implicitly at various appropriate stages in this Manual. The purpose of this Appendix is to make some general points on the subject, and to explain specifically why the various arrangements for wait states were made as they were.

Why have Wait States?

It might be thought foolish to specify and use the "A" version of the Z80-CPU, and run it at its top speed of 4 MHz, then have to slow it down using wait states because it is too fast for some common types of memory device. It might be thought that no net improvement in speed would result. This is not the case, a fact which can be illustrated by analogy: If you have to make a long journey by motor car, which involves a motorway, and a journey through a town, it could be argued that there's no point in having a car which can exceed 30 m.p.h. since that will be the speed limit in the town anyway. If you did use such a car then this would be the equivalent of using a slow non-A version of the Z80-CPU. However most car drivers would agree, that even though a journey through a town has to be restricted to 30 m.p.h. that is no reason to travel at that speed along the motorway as well. To save time you can go as fast as you are permitted along the motorway, and only slow down when you have to. This latter method is the equivalent of using the faster "A" version of the Z80-CPU, and driving flat-out (in the fast dynamic RAM) whenever you get the chance, and only slowing down when you must (e.g. for 450 ns EPROMs). Pushing this analogy further, to shorten the journey in a car it is best to pick a route which avoids the towns as much as possible; this is done in the Interak 1 system by having the ZYMON 2 monitor copy itself out of EPROM and into fast RAM and henceforth running there.

How Do Wait States Work?

The method of wait states is achieved by activating the Z80A-CPU's NWAIT line whenever slow memory is being accessed. This only happens for slow memory because the wait state circuitry is triggered only by a specific block of addresses, i.e. the slow memory addresses; at all the other addresses the wait state circuitry is not activated and the CPU does not slow in the slightest, and of course when it is carrying out all its own internal operations and calculations (which is what a processor is doing continually), it goes at top speed.

Why use a Monostable to Set the Wait States?

Knowledgable users will know that it is possible to use various counts of the Z80A-CPU's own clock to generate predetermined wait states, and this certainly can be more convenient in some designs, as no setting up is required; the wait states are always produced, whether they are needed or not. It is this very predetermination which has persuaded the designers of the LKP-1 card to adopt the adjustable monostable method:

(Appendix 2 continued)

The LKP-1 Card is used as part of a general purpose Interak 1 computer. Although Interak 1 does have some defined features for the convenience of users, these are not forced on to them. Some users for example may be using a much lower clock frequency, for some particular reason, perhaps for e.g. power saving if the new but slower low power Z80L's are in use. Such a user is already suffering reduced performance from his system; the last thing he wants is a fixed extra wait state to be added. The beauty of the monostable method is that it stays fixed to the requirement of the memory devices and does not increase if the CPU clock rate is lowered. The same duration monostable pulse that will cause a wait state at a high frequency will not necessarily cause a wait state at a lower frequency. This is because the duration of the monostable pulse produced is independent of the clock frequency, indeed as are the access time requirements of the memory device.

A further point is that in a general purpose computer it has to be possible to accommodate some memory devices that are ordinarily thought to be obsolete. For example some people have occasional needs to examine or copy programs that are stored in extremely old and very slow EPROMs, with access times measured in microseconds not nano seconds. Such users would find a prewired single wait state clock related system very inconvenient; an LKP-1 user simply increases the number of wait states by adjusting the monostable, or can even use the spare monostable provided to generate very long delays.

Why Not Use Faster Eproms?

There is a lot of sense in this question, because in for example a typical CP/M disk system all of the memory is high speed RAM, and there is just one single "boot EPROM" on the CPU card. In fact for a simple dedicated standard dual floppy disk computer, as used by businessmen etc. this is acceptable; the cost of the single faster EPROM is hardly more than the cost of providing the wait states for a normal speed EPROM. However this solution is not acceptable in Interak 1 because it is also a general purpose work-horse of a computer. Within reason it should be possible for it to satisfy any need of any user. Imagine how you would feel if you had a few hundred EPROMs you wanted to use, and were told you couldn't program or use them in your computer because the designer has cut a few corners on the necessary wait state circuitry; no, the thing has to be designed correctly, or its not worth designing at all - there are plenty of dedicated machines available in the world, Interak has to be very flexible and general purpose.

Other Observations

Although these remarks have been hammering away suggesting that a 4 MHz Z80A-CPU is the only processor to be considered seriously, there are of course numerous other types. Some users may still have much earlier processors such as the 6800, 6802, 6502, SC/MP, and so on, and may not yet be ready to discard them. On the other hand many people will be considering brand new alternatives even to the Z80A. None of

(Appendix 2 continued)

these people would thank the designers of the wait state circuit for producing one which was dedicated specifically to the clock cycle of a 4 MHz Z80A-CPU. The monostable method is entirely general and can be used with any processor which has the same control line as the Z80 NWAIT, i.e. pretty well all processors!

Timing Diagram

A detailed timing diagram is given in Section 5.2 of this Manual. It shows the various waveforms on the standard bus when an access is made to an address which triggers the wait state generation circuit on the LKP-1 card. Although the Z80A-CPU is shown, as stressed above the method works also for numerous different processors.

4.3 APPENDIX 3: LKP-1 APPLICATIONS.

The LKP-1 design is of course dedicated to its fundamental applications (i.e. ASCII Keyboard input, and 4K page select and wait state generation). However there are conceivably other uses, some fairly closely related.

1. Use with Keyboard Encoder Chip.

The generous patch areas on the LKP-1 card can be used to add a keyboard encoder of the user's own choice. For example the (fast disappearing, but once very popular keyboard encoder) type AY-5-2376 can easily be added to the card, and has an output which is compatible with the standard LKP-1 input. The AY-5-2376 has inputs which can be connected to a switch matrix of up to 88 keys (arranged in a particular pattern), and will scan and encode them. This can be useful to take advantage of cheap unencoded keyboards which become available from time to time on the surplus markets.

2. Smaller key arrangements.

Some applications, e.g. "Microprocessor Trainer", or machine tool controllers require only a relatively small number of switches. A "hex. keypad" pehaps, in the former case, and say a start/stop repeat etc. set of buttons and/or limit switches in the latter case.

Two very useful encoder chips which can be used in this type of application are the 74C922 (encodes 16 switches), and 74C923 (encodes 20 switches) either of these is very easy to fit in the space available, and e.g. ribbon cable can be used to connect to the switch matrix.

3. Non-switch Uses.

Devices other than switches can be connected to the LKP-1. For example the output from say a photocell, or say a temperature or smoke detector (provided the signal levels are suitably conditioned).

The LKP-1 input can even be used as a makeshift interface to receive data from another computer. The arrangement of parallel input lines with a strobe is very similar to the method which is used when some computers output data to a printer. The computer in question can be programmed to think it is simply printing on paper, when in fact the printer output is intercepted and redirected to the LKP-1 card. This can also be a useful technique to help diagnose printer problems. If "garbage" is being printed as output from another computer (obviously one inferior to an Interak) then it can be difficult to decide which part of the system is at fault. If the data are fed into the LKP-1 card then they can be stored and analysed at leisure, rather than trying to detect the fault in "real time" inside the printer.

(Appendix 3 continued)

4. Data Logging.

Just as the normal function of the LKP-1 card is to capture parallel keyboard data which may be entered at varying rates, totally unsynchronised with the computer, it can also be so in other applications.

There are a number of processes which generate data at an infrequent random rate, the one which will spring instantly to mind is the detection of cosmic rays in a bubble chamber (sorry to pick such an obvious homely example). At each occurrence it might be vital to gather some data such as which of five laser beams is in operation at the time, and in such a case the cosmic ray detector could be used as the strobe for the data. As the data would then be safely latched the computer could be kept fully occupied in some important calculation and need only "poll" the LKP-1 card at relatively infrequent intervals.

Without the benefit of the latch the computer would have to waste its time "sitting" on the input port, to be sure its attention was not elsewhere at the vital moment.

5. Conversion to Conventional 8-bit Port.

One of the functions of the Interak 1 system (apart from its vital work with laser beams and cosmic rays), is to provide an excellent vehicle to transport inspiration for quick demonstrations into the reality of hardware. If the sudden urge to set up an ordinary 8-bit input port hits you when all the shops are closed, it is an easy matter to improvise something with an old LKP-1 out of your junk box.

In this application U6, U8 and U10 (see circuit diagram sheet 3) may be discarded, and the input lines strapped straight across to U9, the data bus buffer.

6. Use with a 16-bit "Port" Address.

Although the I/O space of the Z80A is commonly thought of as being limited to 256 ports, it should be remembered that it does have the capability of issuing a 16-bit (64K) address during an I/O instruction. For example when the Z80A-CPU executes the input instruction IN r,(C) (i.e. writing data into register r from I/O Port number C) it is well known that whatever value C has is placed on the lower 8 bits of the address bus to provide the I/O Port address. It is not so well known that at this time the upper 8 bits of the address bus contain the contents of the B register, i.e. BC effectively comprises a 16-bit I/O port address. If it is desired to take advantage of this feature for some special system application, then extra decoding devices can be mounted on the patch areas provided. However a most welcome bonus if the 4K page decoder is not in use already is to use it to decode four of the extra address lines,

(Appendix 3 continued)

leaving only 4 needing attention on the patch area circuit. For use in the I/O space the NMREQ and NRFSH lines to the 4K decoder are not needed; they should be replaced by the NIOREQ signal.

7. Use of LKP-1 in the Memory Space.

Sometimes the keyboard port in fairly old-fashioned systems has to be located in the memory space. This could be the case for example in a 6502 type of system (ugh!), since the 6502 CPU does not offer the advantage of a separate I/O Port space.

If a full 16-bit decode is needed to use the LKP-1 card in such a system then, if it is not needed for any other task, the 4K page decoder can be pressed into service to assist, (as in 6 above). This reduces the complexity of any extra decoding circuits required on the patch areas.

8. Adding Wait States to Many Pages.

The 4K page decoder U1, which is used to provide wait states, feeds a three input gate U2a (see sheet 4 of the circuit diagram). This allows the possibility of adding wait states on up to 3 x 4K = 12K of the memory addresses. In a modern high speed RAM-based system this is usually quite sufficient, but for some special application, such as a very EPROM intensive system extra circuitry on the patch areas can be used to add wait states to other addresses as well. This can be a simple arrangement of gates, the output of which can be fed into an unused input of U2a, or alternatively address lines can be removed from the inputs of U1, and the inputs suitably terminated, to turn U1 into say a 3-line to 8-line (8K) decoder, or a 2-line to 4-line (16K) decoder, so as to select ever increasing areas of memory, the select lines being gated together in U2a as before.

9. Differing Wait States.

If the standard wait state setting provided by U5b does not suit all requirements, U5a, the other half of the dual monostable, can be pressed into service, adjusted for some other value. There is already space on the track layout for a timing capacitor between pins 14 and 15, and a resistor from pin 15 to +5V.

10. Other Use for Monostable.

Although it is not the place of the LKP-1 circuit to compromise its performance by attempting to cope with defective keyboards, which generate double characters due to mechanical "bounce" problems, a "fix" might be possible by using the spare half of U5, the monostable.

If you are suffering from a keyboard which can sometimes erroneously generate two or more characters for a single key press, the subsequent

(Appendix 3 continued)

characters can be masked out by taking the strobe through the spare monostable. If the period of the monostable is adjusted to cover the time that the spurious characters are being generated, after the desired character, the unwanted characters will be ignored, as in effect the computer will only detect one strobe (i.e. one character) for the multiple characters generated largely in error.

11. Demonstration Purposes.

As the wait state timing is so eminently adjustable, the LKP-1 wait state generator is excellent for demonstrating the principles for educational purposes. Other educational aspects are discussed in Section 4.4 of this Manual.

12. Use of more than one LKP-1 Card.

It is possible to use more than one LKP-1 card in a system, for example to play some game with several players, e.g. computer "battleships", or alternatively to provide a separate small "hex. keypad" for the convenient entry of data for machine code work, or perhaps setting up data for EPROM programming.

On this last point it is worth pointing out that the Interak 1 computer can be used to make a dedicated EPROM programmer unit with better facilities than commercial units costing a few hundred pounds more than a whole Interak 1 computer. If the conventional full "QWERTY" keyboard is removed and a smaller control panel substituted bearing such legends as "Verify", "Program", etc. the similarity (and the foolishness of buying a dedicated unit) will become clear.

13. Interrupts.

Although in many ways the LKP-1 card already gives a good many of the benefits of an interrupt driven keyboard, (but without any of the software problems), it can be converted to be interrupt driven, but not very easily. Needless to say the patch area would be used, and one of the most convenient ways to add interrupts would be to employ a Z80A-CTC chip, this can be used as a Z80A Mode 2 interrupt controller, by loading one channel to a count of one, and connecting the strobe to the channel input, so that it causes a count down to zero which generates the interrupt. The benefit of using the CTC circuit is mainly that it can hold the Mode 2 interrupt vector, and will also manage the daisy chain priority lines. In addition to the interrupt request line the M1 signal is required from the CPU-card, and the IEI-IEO daisy chain line. All of these signals can be carried on the gold plated edge connector on the "B" side of the card, which is not used in an Interak 1 system. Remember that much more complicated software will be required, and in very high speed protracted applications such as floppy disk access, it will be necessary to think most carefully about the potential loss of disk or keyboard data if a keyboard

(Appendix 3 continued)

interrupt is mismanaged. All in all interrupts are not recommended for the keyboard in an Interak 1 system.

14. Software Note.

One of the main benefits of the LKP-1 card is that it is "latched". This means that the value of any key pressed is saved until the CPU in the system can deal with it. Therefore keys on the keyboard should not be pressed casually, as it is possible to type one character ahead of the computer. This is usually a benefit but it can be a disadvantage; for example, if you are in the middle of an assembly of a long program and you idly press the "Y" key, then if the next question the computer asks when it finishes the assembly is "Shall I destroy everything? Y/N?", it will already have its answer. Needless to say this is only an extreme example; no competent program would be written with a time-bomb like this built in. (To avoid the disaster in the example given, the program should have read the keyboard immediately so as to clear the buffer before asking the question, thus making it impossible for the user to type an answer to the question before it is asked.)

4.4 APPENDIX 4: EDUCATIONAL ASPECTS.

Although the Interak System represents a "real" computer rather than an artificial microprocessor training aid there are some distinct benefits in demonstrating various aspects of digital logic design on such a "real" computer where the student can appreciate that the theoretical techniques, such as truth tables, Boolean logic and the like have some practical application.

If the LKP-1 is used in a Z80A system there is the opportunity on the LKP-1 card to demonstrate various features of the Z80A, such as the separate Memory and I/O spaces, and the use of the NWAIT line.

Of course anyone who has studied this Manual in its entirety will by now have a most comprehensive knowledge of the LKP-1 card, and will also have a distinctly glazed expression, (double glazed if he's read it more than once), but for less dedicated readers a brief summary is given below of various points which can be discussed as part of a training excercise.

For convenience of writing the following discussion points are referenced to the various sheets of the circuit diagram.

Sheet 1. The Block Diagram.

The Diagram Itself: What is a block diagram? How much detail should be included? More importantly, how much should be left off? How much emphasis should be placed on hinting at the precise circuit design? Should only the logical flow be indicated, and the precise circuit implementation be ignored? Should the block diagram be aimed at the knowlegable computer engineer, or a "computer naive"? Could you design the circuit if you were given only a Block Diagram? Can you understand the Block Diagram? If you can't, can you draw a better alternative?

The LKP-1 Design: The Modular system in general, advantages and disadvantages? Should the two functions (Keyboard Port and 4K Page Decoder) which are logically separate be allowed on the same card? What are the "trade-offs"?

Sheet 2. Address Decoder.

Use of pull-up resistor and SPST switch combination where arbitary 0's and 1's are required. Wastage of power in resistor when switched to 0V; alternative?, more expensive switch versus actual cost of power wasted. Note design gives burden of only one LS TTL load per line. See how selected port address is qualified by NIOREQ and NRDS, thus other addresses, writes, and memory addresses ignored. Use of EX-OR gates for comparison of bus address with that preset on switches, (use truth table), can any port be selected? Would decoder for one chosen address only be cheaper? Would it be better, what is benefit of letting user alter it? Note use of wired-OR connection, is really wired-AND logically (ref de Moivres theorem). Stress can only be used with open collector gates, calculate value of pull-ups, minimum/maximum? Show

(Appendix 4 continued)

how diode and resistor logic can carry out open collector function, but resist temptation to do it in practice (because of volt drop across diodes). Address decoder speed, consult TTL Data book - Surprisingly fast, compare with more expensive dedicated address decoders. Remove U7, show that computer still works (assuming it does), why does it? Why is U7 there then? Discuss partial address decoding, tradeoffs, what is best for say "home" computer, what is best for general purpose computer? Run small programs accessing keyboard port, (use a duplicate LKP-1 at a different address for ease of demonstration), examine all waveforms, compare with textbook waveforms, count "T" states, observe bus.

Sheet 3. Data Buffer, Control.

Discuss circuit design (see circuit description earlier in this Manual for description). Demonstrate function of "D" flip-flops, latch, data bus buffer, Schmitt trigger, time constant of power on reset circuit. Discuss ASCII code, observe same actually on pins of latch (run some other program such as 76H, = HALT, to prevent CPU interfering by continually taking the data before you've finished your demonstration).

Sheet 4. 4K Page, Wait States.

Demonstrate function of 4-line to 16-line decoder, by writing suitable demonstration program. Why is NRFSH included? Why isn't NRDS and NWDS? Note inputs to U2a are pulled high by R1-R3, when inputs not used. Why doesn't the pull up resistor conflict with the output from the page decoder when it goes low? Explain difference in currents and voltages for TTL logic 0 compared with logic 1. Why are R1-R3 10k, when R5, another pull-up, is 1k? Run program giving continuous access of a selected 4K page. Show the precise effect of the NWAIT line, compare with Z80 textbook timing diagrams. Observe monostable operation. Consult TTL databook for theoretical monostable pulse width, measure in practice, using oscilloscope. Point out inaccuracy of 'scope calibration, measure again using an accurate digital timer and compare with 'scope reading, remember percentage tolerance on components. Discuss use of open-collector driver on NWAIT line.

Incidentally, all 'scope readings, show how moving earth clip on probe alters waveshape; does 'scope really show the truth? Observe and measure propogation delays, compare with TTL databook expectations.

Sheet 5. Decoupling Capacitors.

What are decoupling capacitors? Why are they there, why bother with numerous small ones when an electrolytic is present? Calculate impedance of even a short length of wire at high frequencies (estimate the inductance of the wire, does anyone remember the formula?).

(Appendix 4 continued)

Project

If spare LKP-1 cards are available carry out a conversion to make one into a general purpose input port. (This is an excercise in understanding; there is much more intellectual benefit to be gained in working out whether or not to leave in a latch, which connections to break, which to make and so on, than just the "dumb" connection to an ordinary computer input port.)

Are there any other applications for an unmodified LKP-1 card, in addition to its use with an ASCII keyboard? How about measurements of "random" phenomena, which might be missed if the CPU wasn't looking in the right place at the right time?

4.5 APPENDIX 5: COMPARISON BETWEEN KEMITRON DCR-6 AND INTERAK LKP-1.

The Kemitron DCR-6 Card provided the same function some years ago as the Interak LKP-1 card does today. As the DCR-6 was designed such a long time ago, in fact before the Z80A-CPU was generally available, it suffered some disadvantages. The purpose of this Appendix is to provide information to those users who have a Kemitron DCR-6 card and are thinking of changing to the Interak alternative. Although for convenience the points will be made in the form of disadvantages attached to the DCR-6 and advantages attached to the LKP-1, this should not be taken to imply any criticism of the original Kemitron card, it was just simply designed at a time when the Z80A was unforseen, and it was inconceivable that anyone could afford more than a few K of RAM!

Disadvantages of Kemitron DCR-6 when used in an Interak 1 System

1. Only the first ten of the possible 16 "4K Page Selects" were provided - this means that Page F (i.e. the VDU Address) cannot be reached without modifying the board.

2. The Page Selects provided did not include the NMREQ signal in the decoding - i.e. modification was needed if the separate memory and I/O spaces were employed in the system (e.g. particularly with the Z80).

3. No specific I/O Port decoding was provided. The DM 8131 device, as well as being not commonly known, had insufficient inputs to decode the 8-bit I/O Port Address, also the NIOREQ signal was not included in the decoding.

4. The 4-bit latch, controlled by the SC/MP "NADS" signal, was rapidly becoming redundant on the DCR-6 card:

   a. Because SC/MP was going out of fashion.

   b. Because the SC/MP cards which did not have the latch were being discontinued by Kemitron, and their current replacements already had the latch on board.

   c. A monostable was needed on the DCR-6 card to "stretch" the strobe from the keyboard, so that the CPU was more able to "catch" a key which was pressed on the keyboard. This was fine when the CPU was idling in a "polling" loop, but when it was busy executing programs of other sorts, repeated keystrokes were required to break into the programs.

(Appendix 5 continued)

An increased monostable duration increased the chances of a keystroke being "caught" by the CPU in such circumstances, but there was a limit to how much the duration could be increased:

a. Because some software would loop back and read the same key again, giving an effect similar to keyboard "bounce".

b. Because very fast keystrokes rates would be ignored if subsequent ones were "masked " by the strobe of the first.

It was therefore felt that a "latched" keyboard interface would offer some significant advantages. (The "ultimate" method - an interrupt driven keyboard - was not adopted, because not all existing hardware, nor software, can handle interrupts. It would be unfair to expect existing users to have much of their present systems rendered obsolete.)

Advantages of LKP-1 Design

1. The 74LS154 4-line to 16-line decoder provides all 16 "4K Page Selects", and includes provision for the NMREQ signal. (Note that the last remaining Kemitron card which required the provision of a page select signal was the VDU-G; new users of the replacement VDU-K will know that this does not require that a page select signal be provided.)

2. An 8-bit I/O Port decoder, which includes the necessary NIOREQ bus signal, is included. An optional 8xSPST DIL switch lets any one of the possible 256 ports be used for the keyboard.

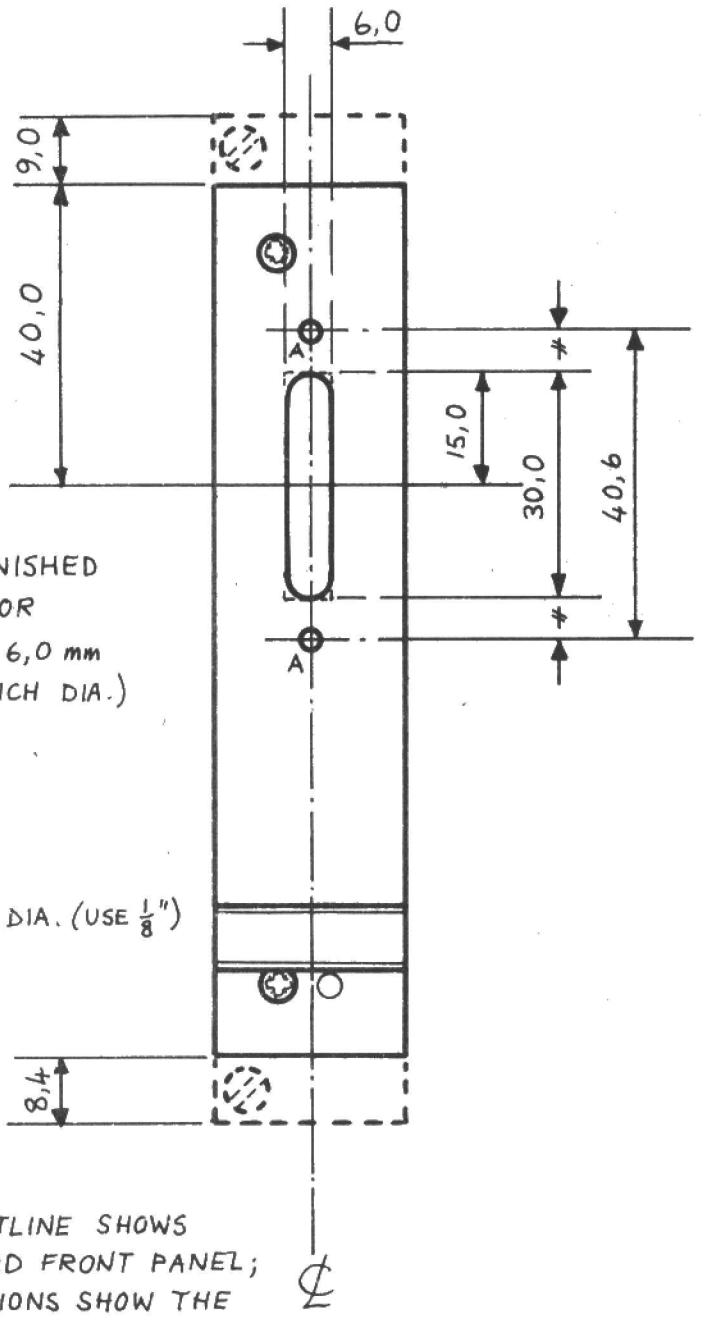
3. The data from the keyboard are held latched on the LKP-1 card, and are automatically cleared when the CPU reads the keyboard port. Provision has been made to avoid possible incorrect reading in the (admittedly unlikely) event of a strobe from the keyboard being received at the very moment a CPU read of the LKP-1 card is in progress - if the strobe is not present at the start of the read cycle it is automatically delayed until the next read cycle.

5.1 LKP-1 BUS ALLOCATIONS (Note "B" side not used)

1A.	NIOREQ	I/O Request
2A.	NMREQ	Memory Request
3A.	(NWDS)	(Write Data Strobe)
4A.	NRDS	Read Data Strobe
5A.	AB15	Address Bus
6A.	AB14	Address Bus
7A.	AB13	Address Bus
8A.	AB12	Address Bus
9A.	(AB11)	(Address Bus)
10A.	(AB10)	(Address Bus)
11A.	(AB9)	(Address Bus)
12A.	(AB8)	(Address Bus)
13A.	AB7	Address Bus
14A.	AB6	Address Bus
15A.	AB5	Address Bus
16A.	AB4	Address Bus
17A.	AB3	Address Bus
18A.	AB2	Address Bus
19A.	AB1	Address Bus
20A.	AB0	Address Bus
21A.	NRST	Reset
22A.	DB7	Data Bus
23A.	DB6	Data Bus
24A.	DB5	Data Bus
25A.	DB4	Data Bus
26A.	DB3	Data Bus
27A.	DB2	Data Bus
28A.	DB1	Data Bus
29A.	DB0	Data Bus
30A.	(N1IN)	(Daisy Chain)
31A.	(N1OUT)	(Daisy Chain)
32A.	NRFSH	Dynamic RAM Refresh
33A.	(ϕ)	(4.0 MHz Z80A Clock)
34A.	NWAIT	Wait State Request
35A.	(+12V)	(Power Supply)
36A.	(+12V)	(Power Supply)
37A.	Pol	Polarisation Slot
38A.	(-12V)	(Power Supply)
39A.	(-12V)	(Power Supply)
40A.	0V	Power Supply
41A.	0V	Power Supply
42A.	+5V	Power Supply
43A.	+5V	Power Supply

Signals named in brackets are not used by the card; NRFSH on A32 is used but need not be connected in systems which have no signal on this line; in such circumstances the line should be connected to a logic "1". For KBUS-12, the NWAIT line should be transferred to A30. The -12V supply is routed to the keyboard connection area in case the keyboard requires it, the LKP-1 card itself needs only 5V.

FEATURES NOT DIMENSIONED ARE ALREADY PRESENT ON THE STANDARD 1 INCH METAL FRONT PANELS.



THE SLOT CAN BE FINISHED WITH SQUARE ENDS, OR ROUNDED (E.G. USE 6,0 mm DIA. DRILL, OR 7/32 INCH DIA.)

2 'A' HOLES 3,10 DIA. (USE 1/8")

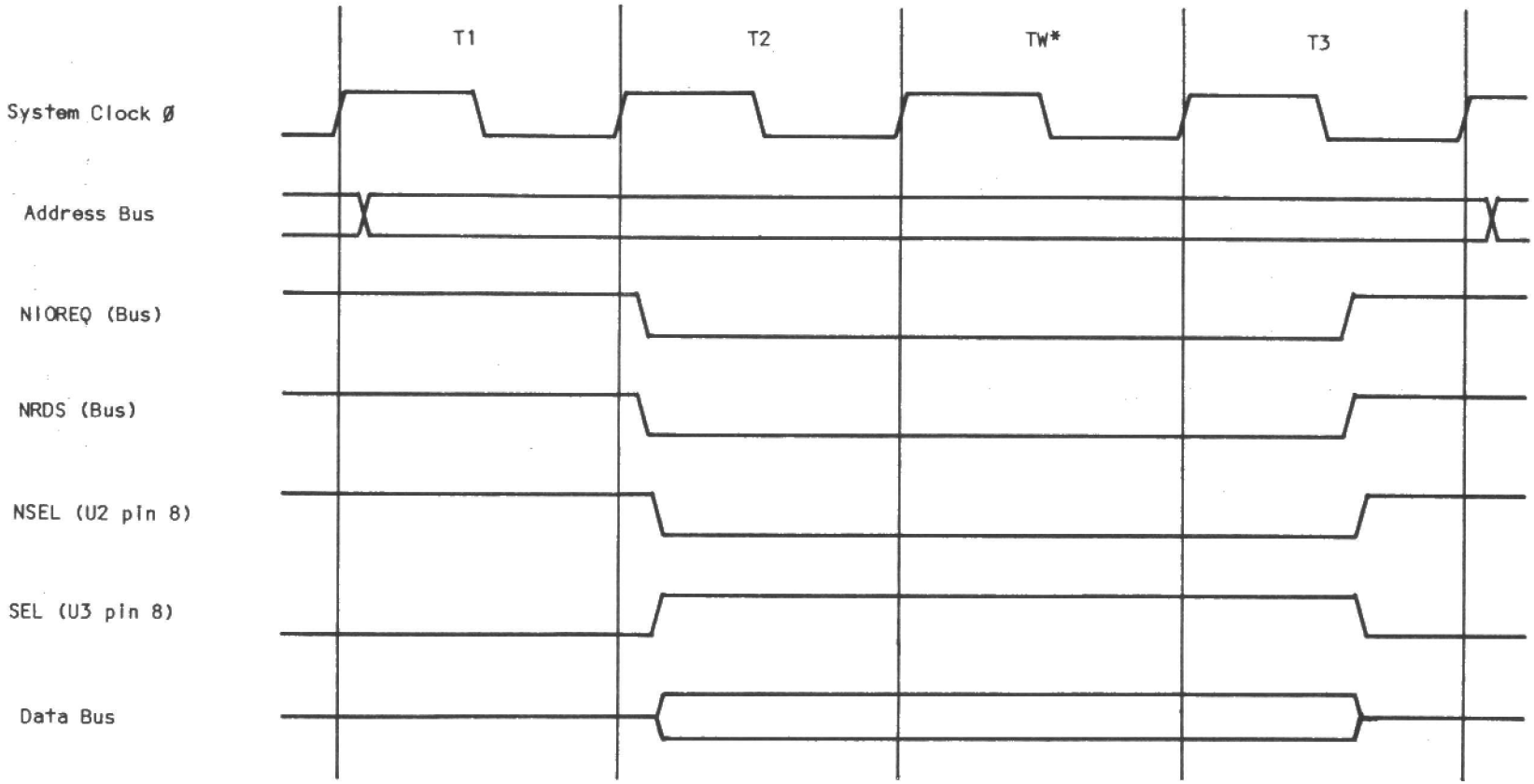
NOTE: THE SOLID OUTLINE SHOWS THE "NEW TYPE" CARD FRONT PANEL; THE DOTTED EXTENSIONS SHOW THE "OLD (R.S.) TYPE".

Drawn	D.M.P
Date	9-5-83
Scale	1:1
Dims.	mm

Interak

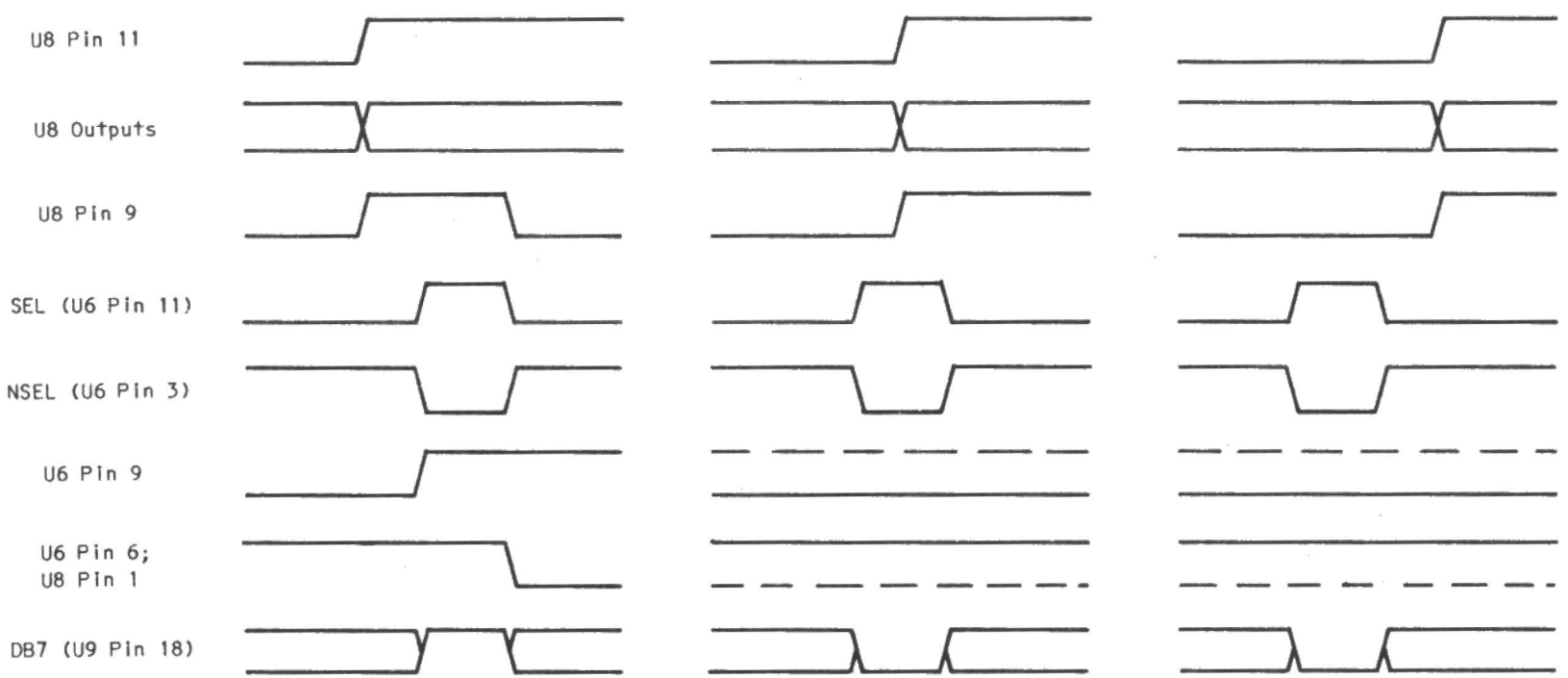
LKP-1 FRONT PANEL DRILLING ETC. DETAILS

1 OF 1



*This Wait state is inserted by the CPU for all Port Reads

	Drawn D.M.P	Interak
	Date 16-5-83	LKP-1 TIMING DIAGRAMS, SHEET 1: KEYBOARD PORT READ
	Scale 1µs = 160mm	1 OF 3



KEY PRESSED BEFORE SEL - DATA ACCEPTED.

KEY PRESSED DURING SEL - DATA REJECTED. (Will be read next time.)

KEY PRESSED AFTER SEL - DATA REJECTED. (Will be read next time.)

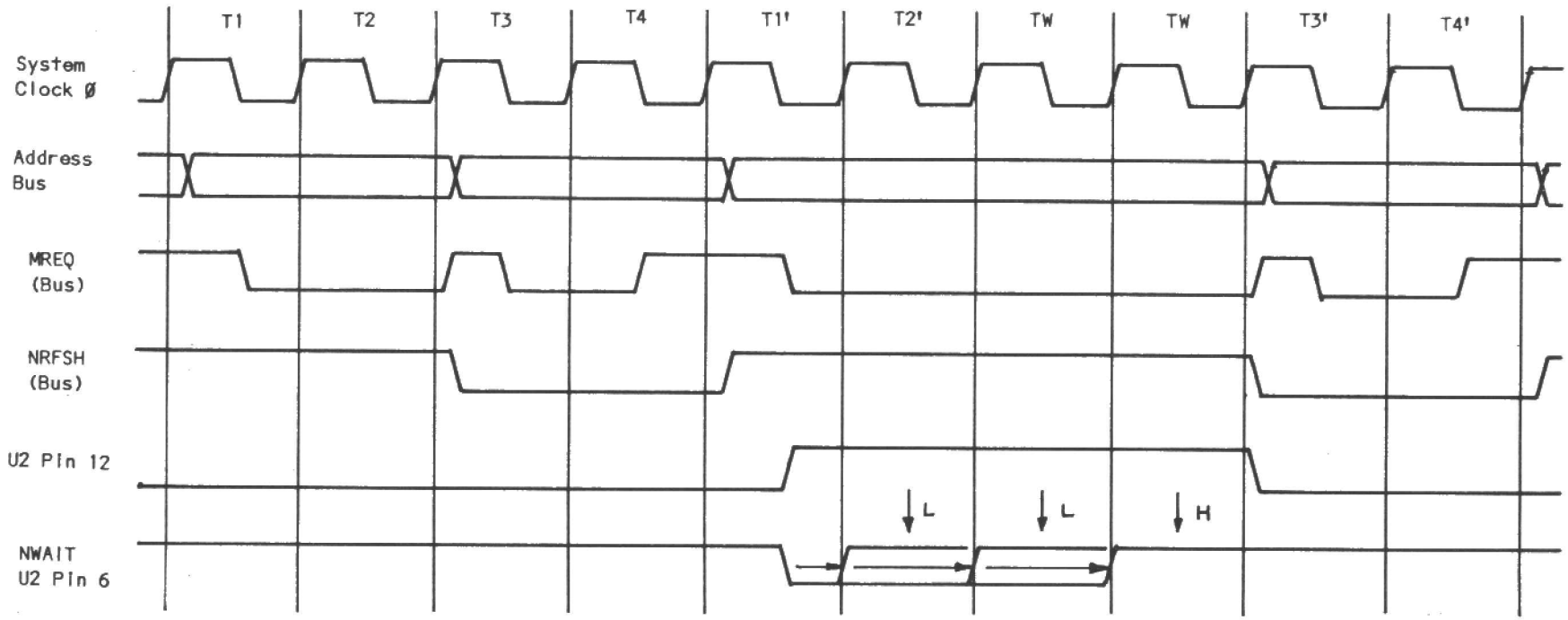
(Refer to Circuit Diagram Sheet 3)

Drawn	D.M.P.
Date	16-5-83
Scale	1μs = 24 mm

Interak

LKP-1 TIMING DIAGRAMS, SHEET 2; READ SYNCHRONISATION FLIP-FLOP

2 OF 3



(Monostable Period)

No. of Wait States 0 1 2

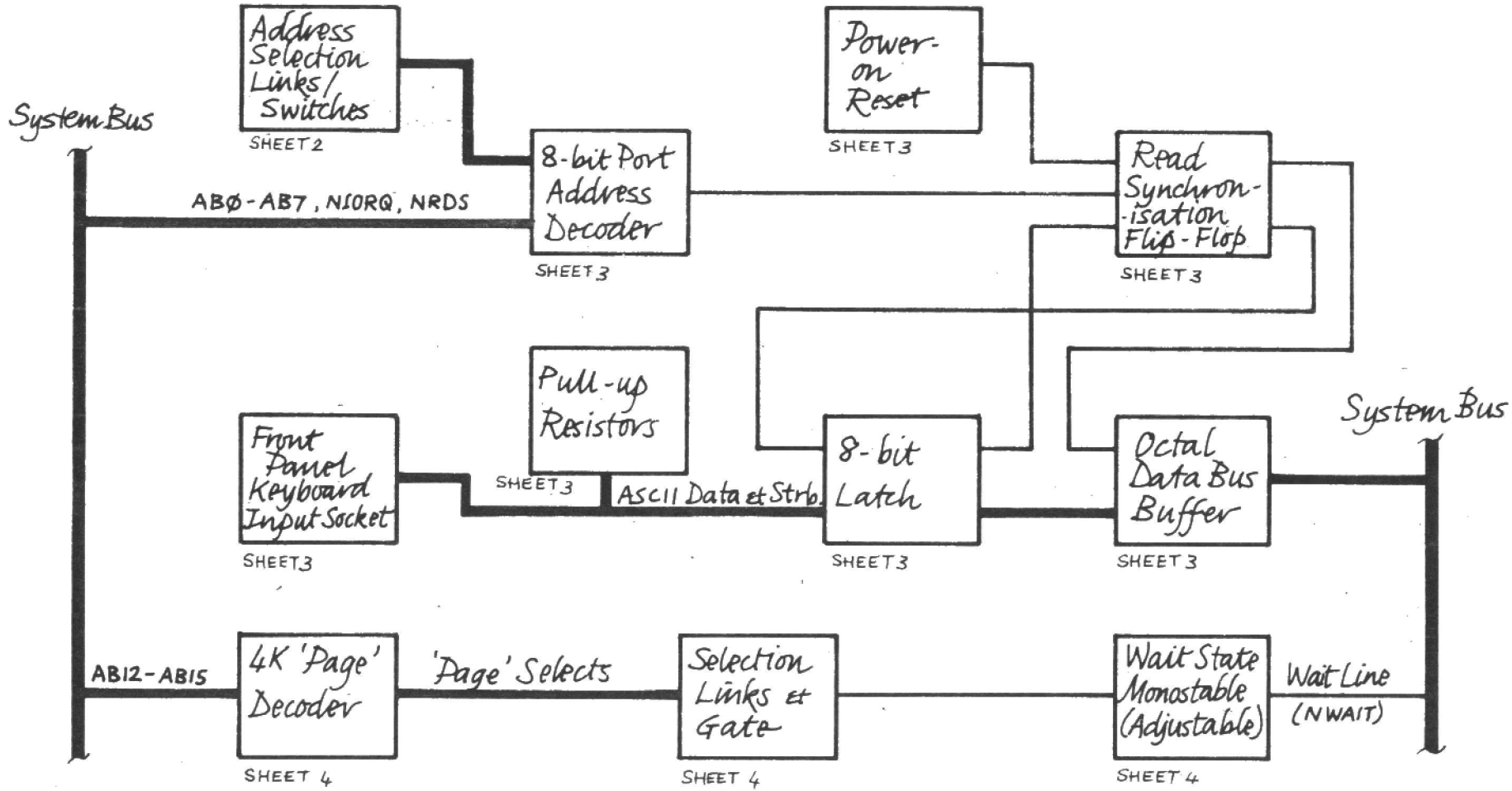
The diagram shows 2 ficticious "M1" (Op-code Fetch) cycles. The first cycle (T1, T2, T3, T4) is one where no wait states have been selected; the second (T1', T2', TW, TW, T3', T4') is from memory where wait states have been selected.

Drawn	D.M.P.
Date	16-5-83
Scale	1µs = 80mm

Interak

LKP-1 TIMING DIAGRAMS, SHEET 3: 4K PAGE WAIT STATE MONOSTABLE

3 OF 3



(KEY TO SYMBOLS USED IN CIRCUIT DIAGRAMS, POWER SUPPLIES, DECOUPLING CAPACITORS:- - SHEET 5)

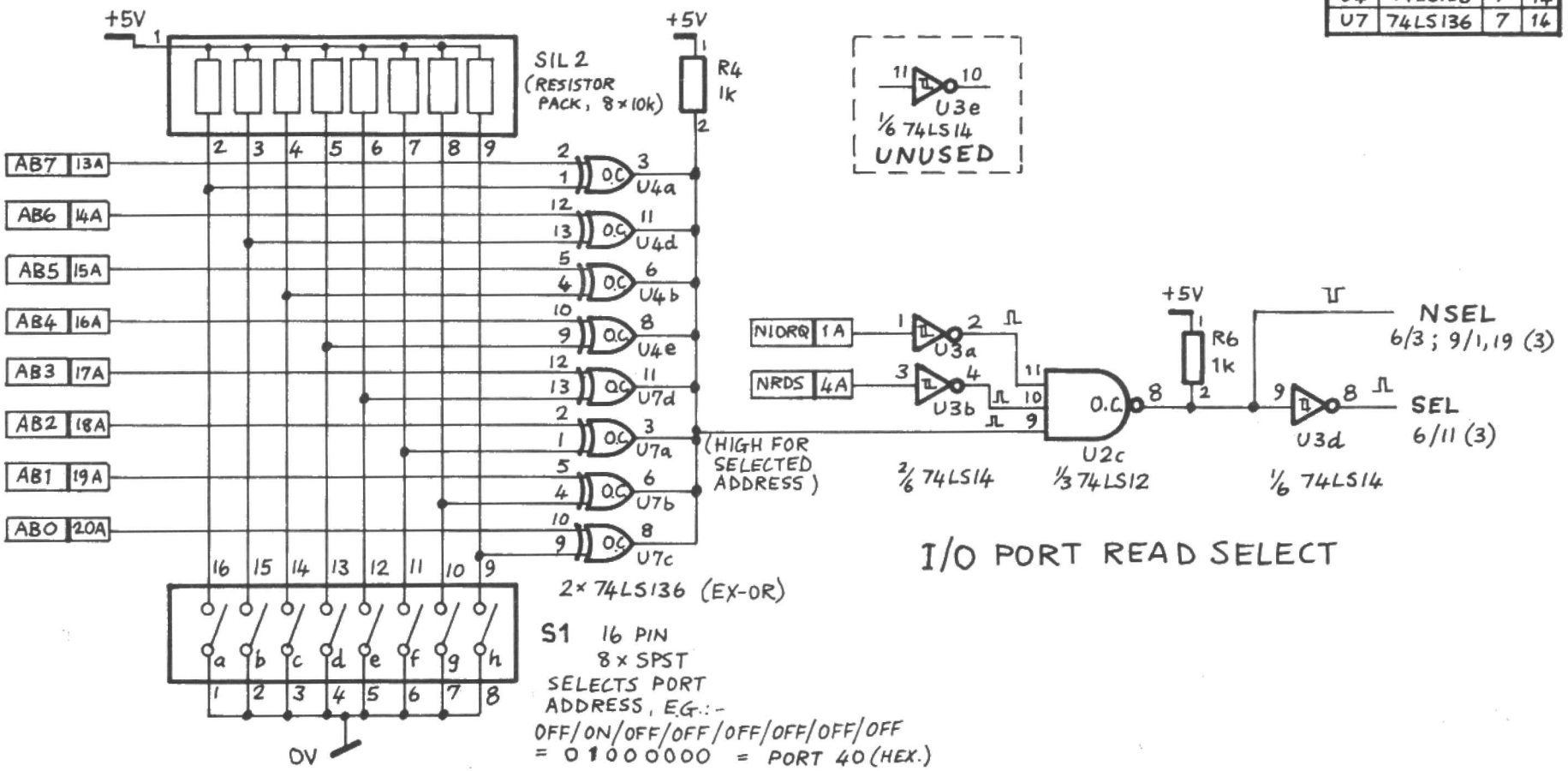
Drawn	D.M.P
Date	9-5-83
Scale	-

Interak

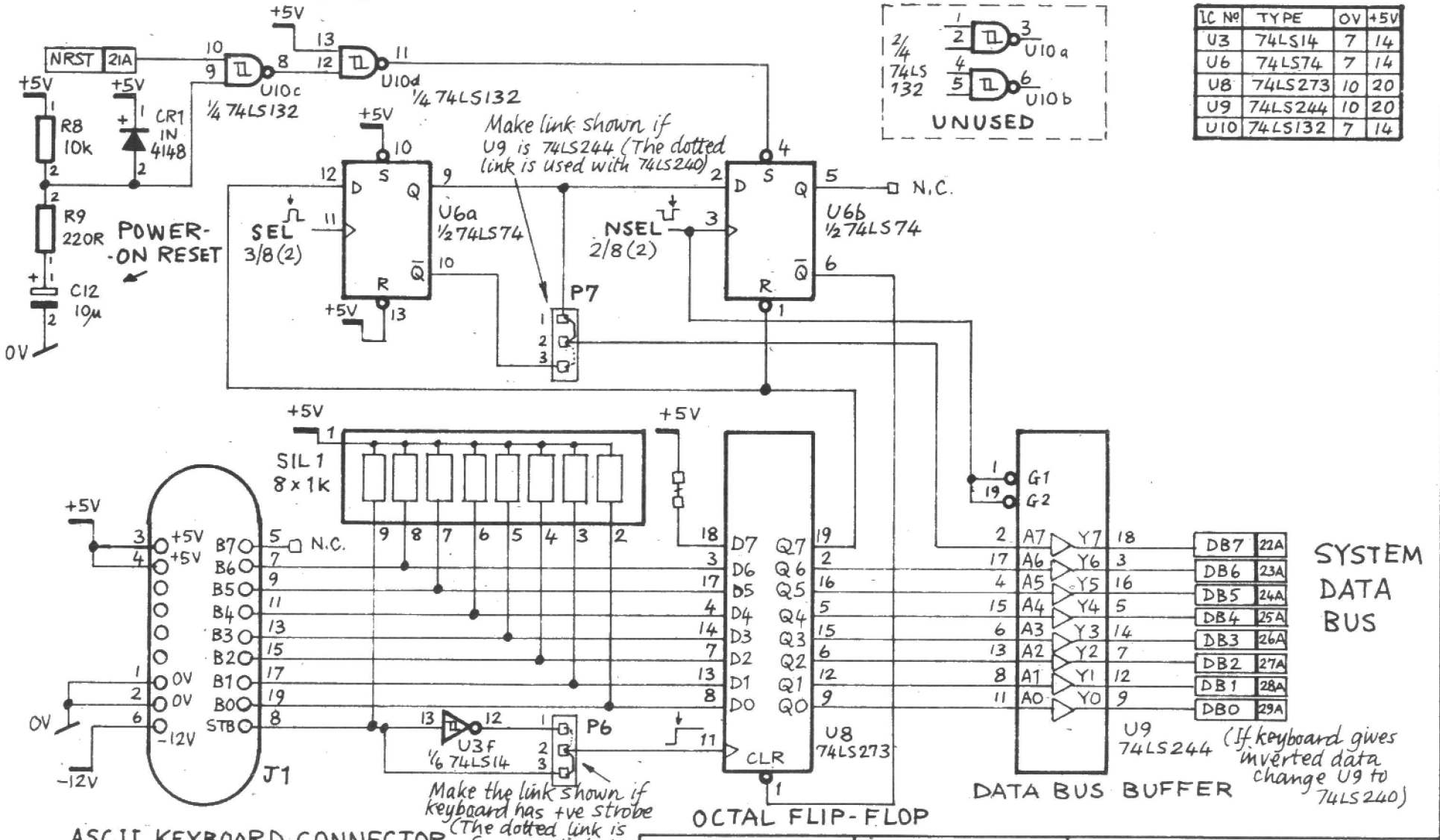
LKP-1 CIRCUIT DIAGRAM, SHEET 1: BLOCK DIAGRAM

1 OF 5

IC No	TYPE	0V	+5V
U2	74LS12	7	14
U3	74LS14	7	14
U4	74LS136	7	14
U7	74LS136	7	14



	Drawn D.M.P.	Interak
	Date 9-5-83	LKP-1 CIRCUIT DIAGRAM, SHEET 2
	Scale -	PORT ADDRESS COMPARATOR
		2 OF 5



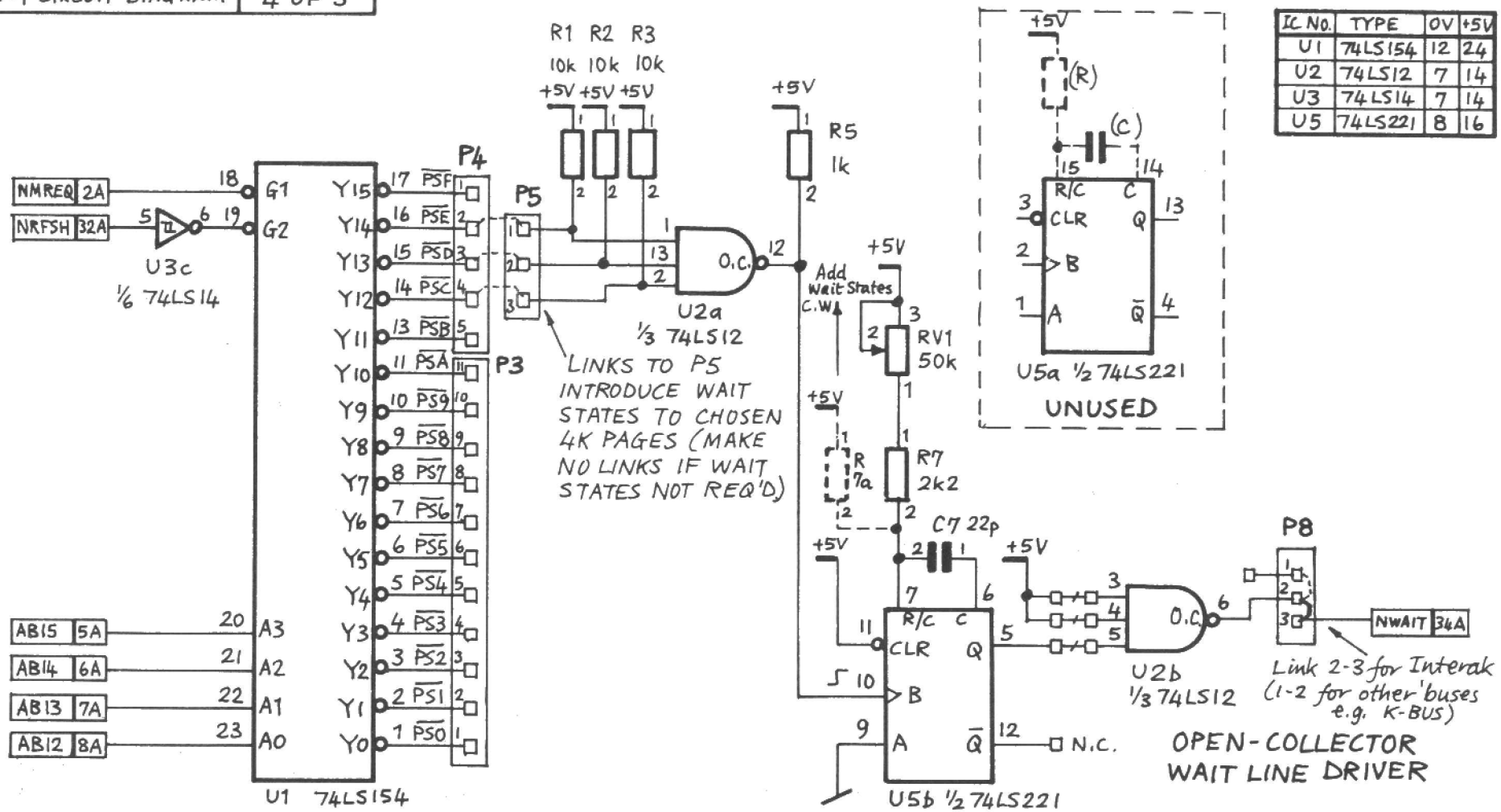
IC No	TYPE	0V	+5V
U3	74LS14	7	14
U6	74LS74	7	14
U8	74LS273	10	20
U9	74LS244	10	20
U10	74LS132	7	14

Drawn	D.M.P
Date	9-5-83
Scale	-

Interak

LKP-1 CIRCUIT DIAGRAM, SHEET 3
DATA INPUT, BUFFER CONTROL,
POWER-ON RESET

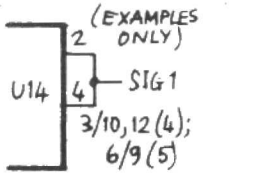
3 OF 5



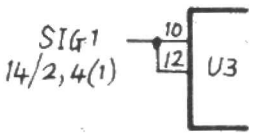
IC No.	TYPE	0V	+5V
U1	74LS154	12	24
U2	74LS12	7	14
U3	74LS14	7	14
U5	74LS221	8	16

Drawn	D.M.P	Interak
Date	9-5-83	LKP-1 CIRCUIT DIAGRAM, SHEET 4: 4K PAGE SELECTS, WAIT STATE MONOSTABLE
Scale	-	4 OF 5

KEY TO SYMBOLS USED ON CIRCUIT DIAGRAMS



OUTPUT PINS 2 AND 4 OF U14 PRODUCE A SIGNAL CALLED SIG1, WHICH IS CONNECTED TO U3 PINS 10, 12 (SHEET 4); AND U6 PIN 9 (SHEET 5).



INPUT PINS 10 AND 12 OF U3 RECEIVE A SIGNAL CALLED SIG1 WHOSE SOURCE IS U14 PINS 2,4 (SHEET 1)

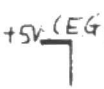
0.1" PITCH EDGE CONNECTOR POSITION EG A2 IS SIDE A, PIN 2; B3 IS SIDE B PIN 3, ETC. BUS SIGNAL NAME.

CONNECTION PAD OR PIN.

POSITION WHERE TRACK MAY BE CUT FOR SOME SPECIAL PURPOSE, ALTERNATIVE CONNECTION SHOWN DOTTED.

WIRE LINK (EG WIRE WRAPPED TO TERMINAL PINS) SHOWN SOLID. ALTERNATIVE POSITION SHOWN DOTTED

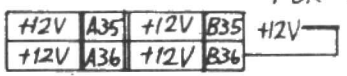
0V, EARTH CONNECTION



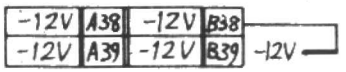
CONNECTION TO NAMED POWER SUPPLY RAIL

POWER SUPPLIES

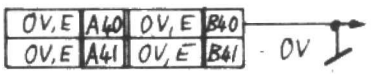
(EDGE CONNECTOR PINS A37, B37 REMOVED FOR POLARISING KEY)



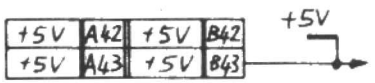
+12V NOT USED ON THIS CARD.



-12V POWER RAIL.



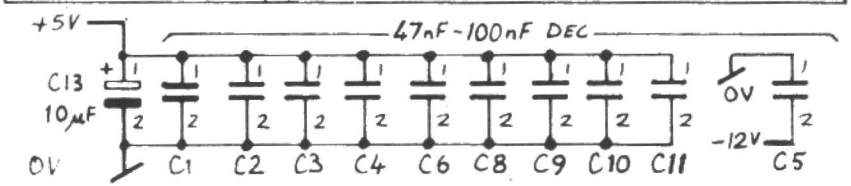
0V, EARTH POWER RAIL.



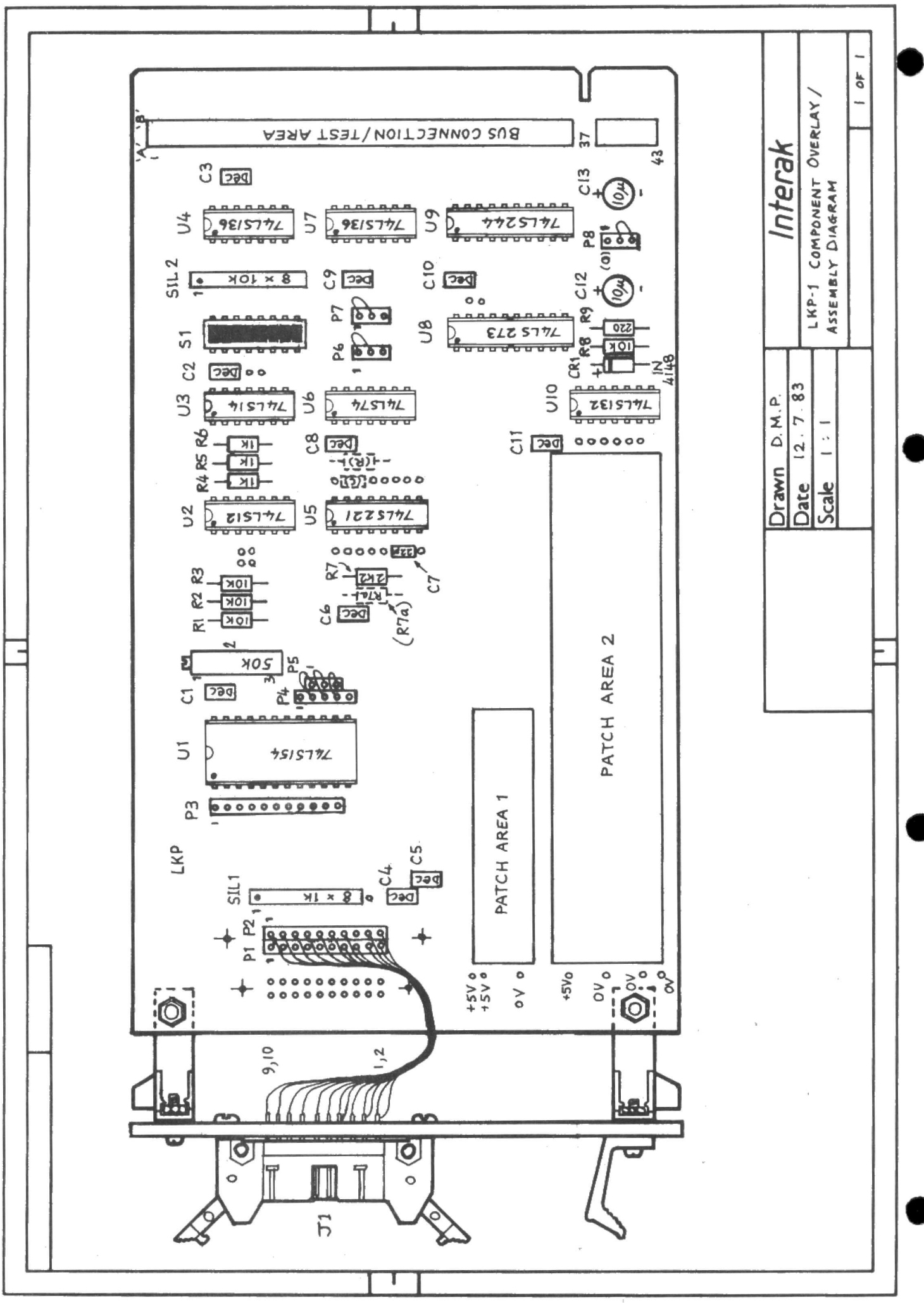
+5V POWER RAIL.

IC POWER SUPPLY CONNECTIONS ARE LISTED IN A TABLE IN ONE CORNER OF EACH SHEET OF THE MAIN CIRCUIT DIAGRAMS. FOR CLARITY OF LOGIC FLOW THE POWER SUPPLY CONNECTIONS ARE NOT NORMALLY INCLUDED ON THE GRAPHIC PART OF THE CIRCUIT DIAGRAMS. CONNECTIONS TO THE POWER SUPPLY RAILS FOR OTHER PURPOSES (E.G. ENABLES, DISABLES ETC.) ARE SHOWN.

DECOUPLING CAPACITORS



	Drawn D.M.P	Interak
	Date 9.11.82	LKP-1 CIRCUIT DIAGRAM, SHEET 5: KEY TO SYMBOLS, AND POWER SUPPLIES
	Scale -	5 OF 5


BUS CONNECTION/TEST AREA
PATCH AREA 1
PATCH AREA 2
LKP
SIL1
SIL 2
P1 P2
P3
P4
P5
P6
P7
P8
S1
J1
9,10
1,2
+5V
+5V
0V
+5V
0V
0V
0V
74LS154
74LS14
74LS12
74LS74
74LS221
74LS273
74LS244
74LS136
74LS132
50K
8 x 10K
8 x 1K
10K
1K
2K2
220
10µ
Dec
IN 4148
Interak
LKP-1 COMPONENT OVERLAY / ASSEMBLY DIAGRAM
Drawn D.M.P.
Date 12.7.83
Scale 1:1
1 OF 1

COMPONENT PARTS LIST FOR LKP-1 CARD

Issue 4 Date: April 1983

LISTED BY COMPONENT REFERENCE NUMBER

Resistors 0.25W (0.5" pitch)

R1	10k	0.5"	R6	1k	0.5"
R2	10k	0.5"	R7	2k2	0.5"
R3	10k	0.5"	R8	10k	0.5"
R4	1k	0.5"	R9	220R	0.5"
R5	1k	0.5"			

SIL Resistors (Use Sockets)

SIL1 9-pin 8x1k
SIL2 9-pin 8x10k

Variable Resistor (Multiturn Type)

RV1 50k

Capacitors

C1	Dec	0.2"	C8	Dec	0.2"
C2	Dec	0.2"	C9	Dec	0.2"
C3	Dec	0.2"	C10	Dec	0.2"
C4	Dec	0.2"	C11	Dec	0.2"
C5	Dec	0.2"	C12	10µ Al	0.2"
C6	Dec	0.2"	C13	10µ Al	0.2"

C7 22p Cer (5% tolerance) 0.1"

"Cer" = Ceramic
"Dec" = 47-100n Decoupling grade polyester, or Ceramic
"Al" = Low Leakage Min. Aluminium

Diode

CR1 1N4148 0.5"

Integrated Circuits (Use Sockets)

U1	74LS154	(24)	U6	74LS74	(14)
U2	74LS12	(14)	U7	74LS136	(14)
U3	74LS14	(14)	U8	74LS273	(20)
U4	74LS136	(14)	U9	74LS244	(20)
U5	74LS221	(16)	U10	74LS132	(14)

0.1" Pitch Pin Assemblies

P1	5-pin + 5-pin	P5	3-pin
P2	5-pin + 5-pin	P6	3-pin
P3	5 + 3 + 3-pin	P7	3-pin
P4	5-pin	P8	3-pin

LISTED BY COMPONENT VALUE

Resistors 0.25W (0.5" pitch)

220R	1	R9	(0.5")
1k	3	R4,5,6	(0.5")
2k2	1	R7	(0.5")
10k	4	R1,2,3,8	(0.5")

SIL Resistors (Use Sockets)

SIL1 9-pin 8x1k
SIL2 9-pin 8x10k

Variable Resistor (Multiturn)

50k 1 RV1

Capacitors

22p	Cer	1	C7 (5% tolerance)
Dec		10	C1-6,8-11
10µ	Al	2	C12,13

"Cer" = Ceramic
"Dec" = 47-100n Decoupling grade polyester, or Ceramic
"Al" = Low Leakage Min. Aluminium

Diode

1N4148 1 CR1 (0.5")

Integrated Circuits (Use Sockets)

74LS12	1	U2	(14 pin)
74LS14	1	U3	(14 pin)
74LS74	1	U6	(14 pin)
74LS132	1	U10	(14 pin)
74LS136	2	U4,7	(14 pin)
74LS154	1	U1	(24 pin)
74LS221	1	U5	(16 pin)
74LS244	1	U9	(20 pin)
74LS273	1	U8	(20 pin)

0.1" Pitch Pin Assemblies

3 pin	6	P3,3',5-8
5 pin	6	P1,1',2,2',3,4

COMPONENT PARTS LIST FOR LKP-1 CARD (continued)

DIL & SIL Sockets

9-pin SIL	2	SIL1,2	20-pin DIL	2	U8,9
14-pin DIL	6	U2,4,6,7,10	24-pin DIL	1	U1
16-pin DIL	2	S1; U5			

Sundry

Pre-stripped Insulated Wire (Including some spares)
10 off 25mm (for links)
*20 off 76mm (for connecting J1 to card)

Switches
*S1 16-pin 8xSPST

PCB and Manual
*LKP-1 p.c.b, sold separately as "LKP-1 Bare Board"
*Manual, sold separately as "LKP-1 Manual"

Card Front
*1 off Kit (1 inch wide) including fixings and mounting brackets, new type or old (RS) type, according to type of rack used.

Note Options: The items marked "" in the parts lists are not supplied in the standard kit of parts for the LKP-1; however they are available separately, as indeed are all the components.

Resistor Colour Code (Ignore last band (generally gold))
220R Red, Red, Brown
1k Brown, Black, Red
2k2 Red, Red, Red
10k Brown, Black, Orange